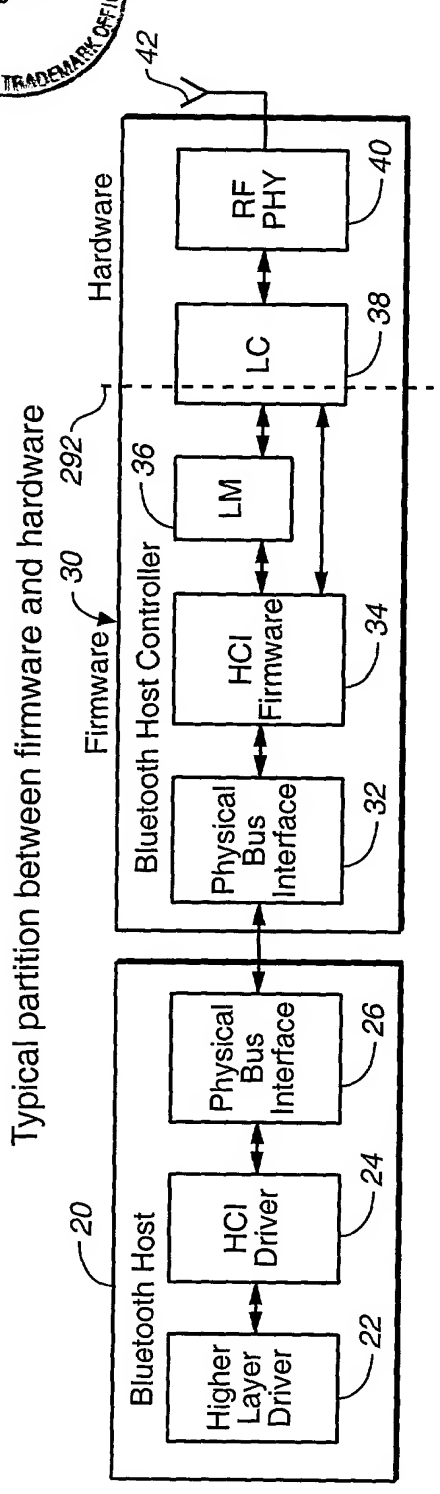


FIG._1
(PRIOR ART)

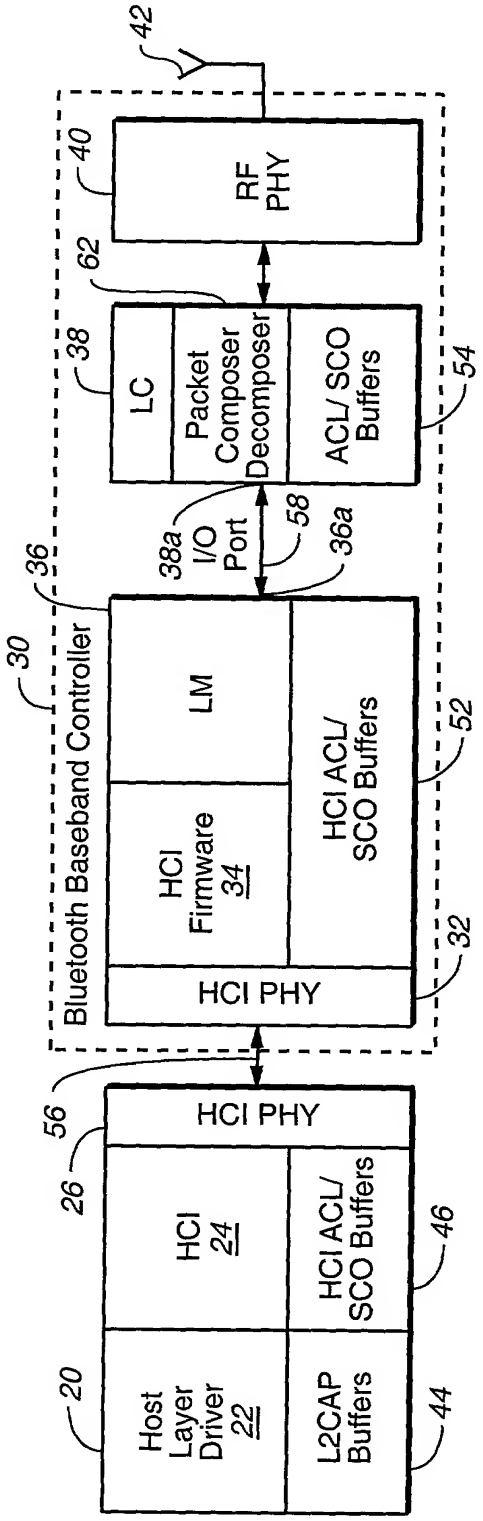


FIG._2
(PRIOR ART)

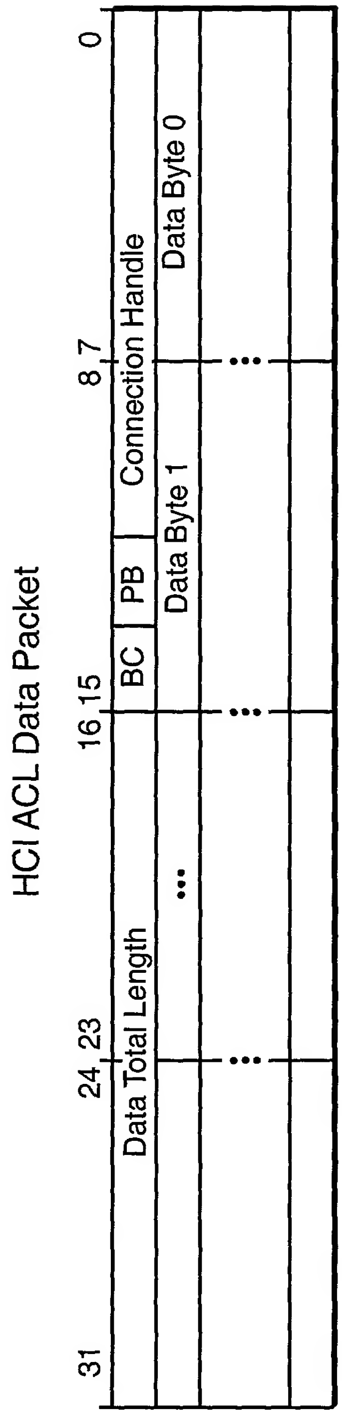


FIG._3A
(PRIOR ART)

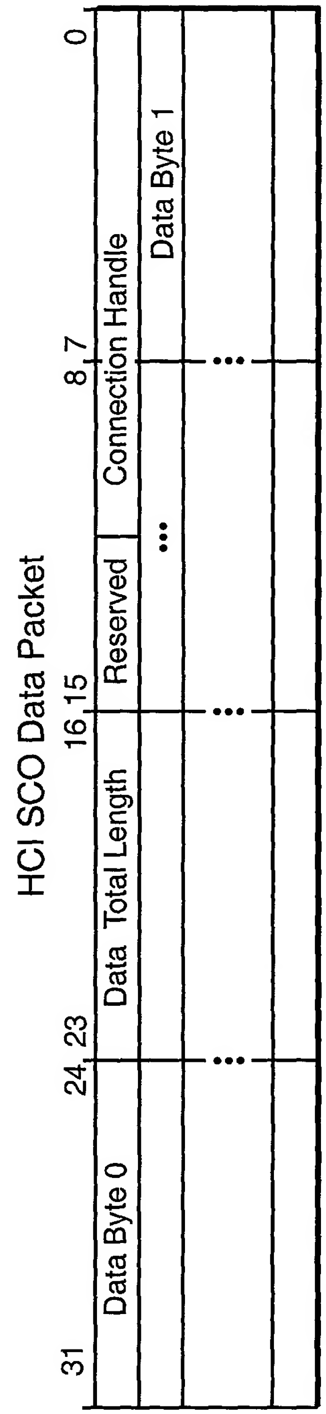


FIG._3B
(PRIOR ART)

Data Flow and Buffer Scheme in the Bluetooth Host Controller

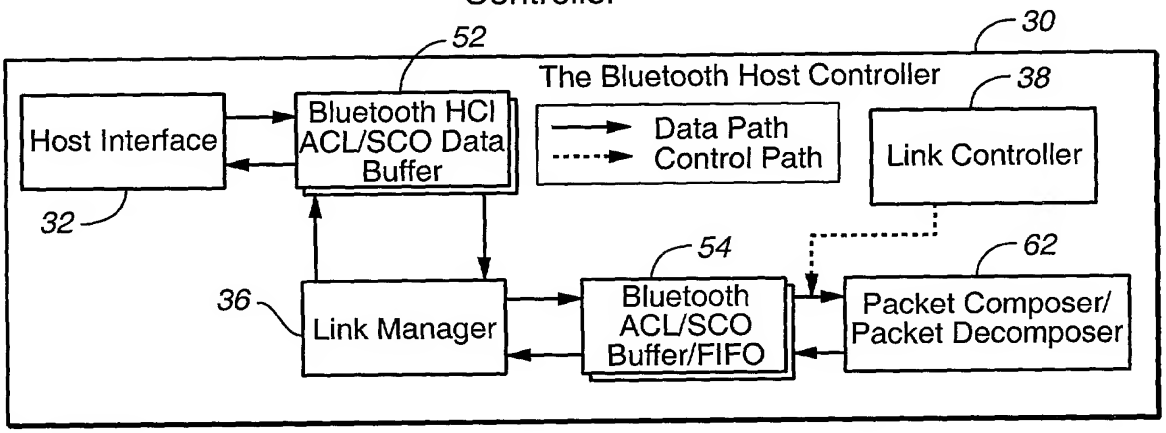


FIG._4
(PRIOR ART)

Dual Buffer Scheme For ACL Packet Transmission

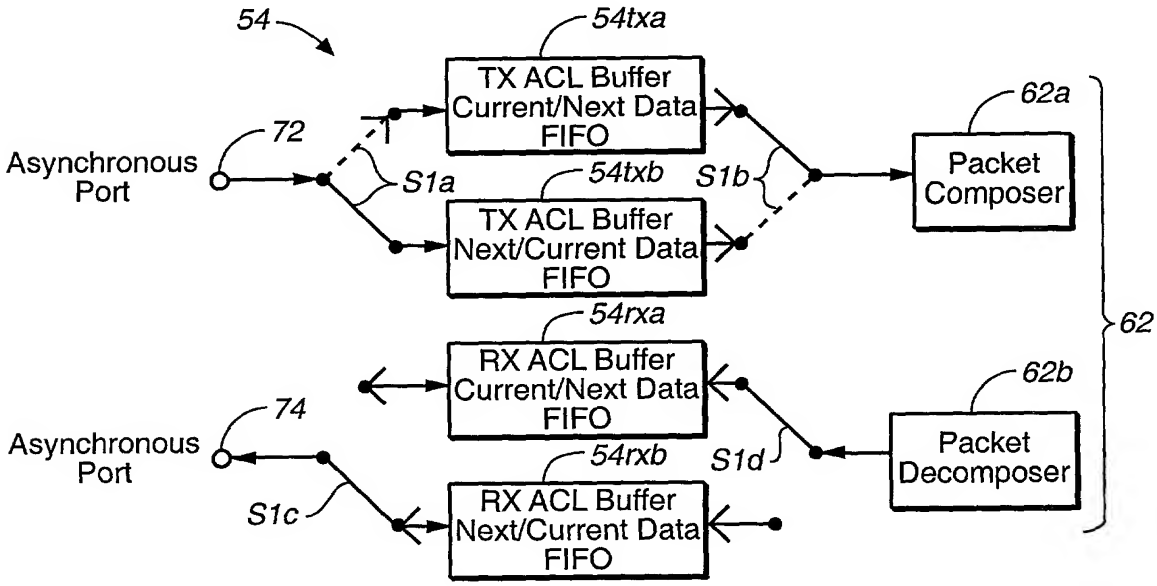


FIG._5A
(PRIOR ART)

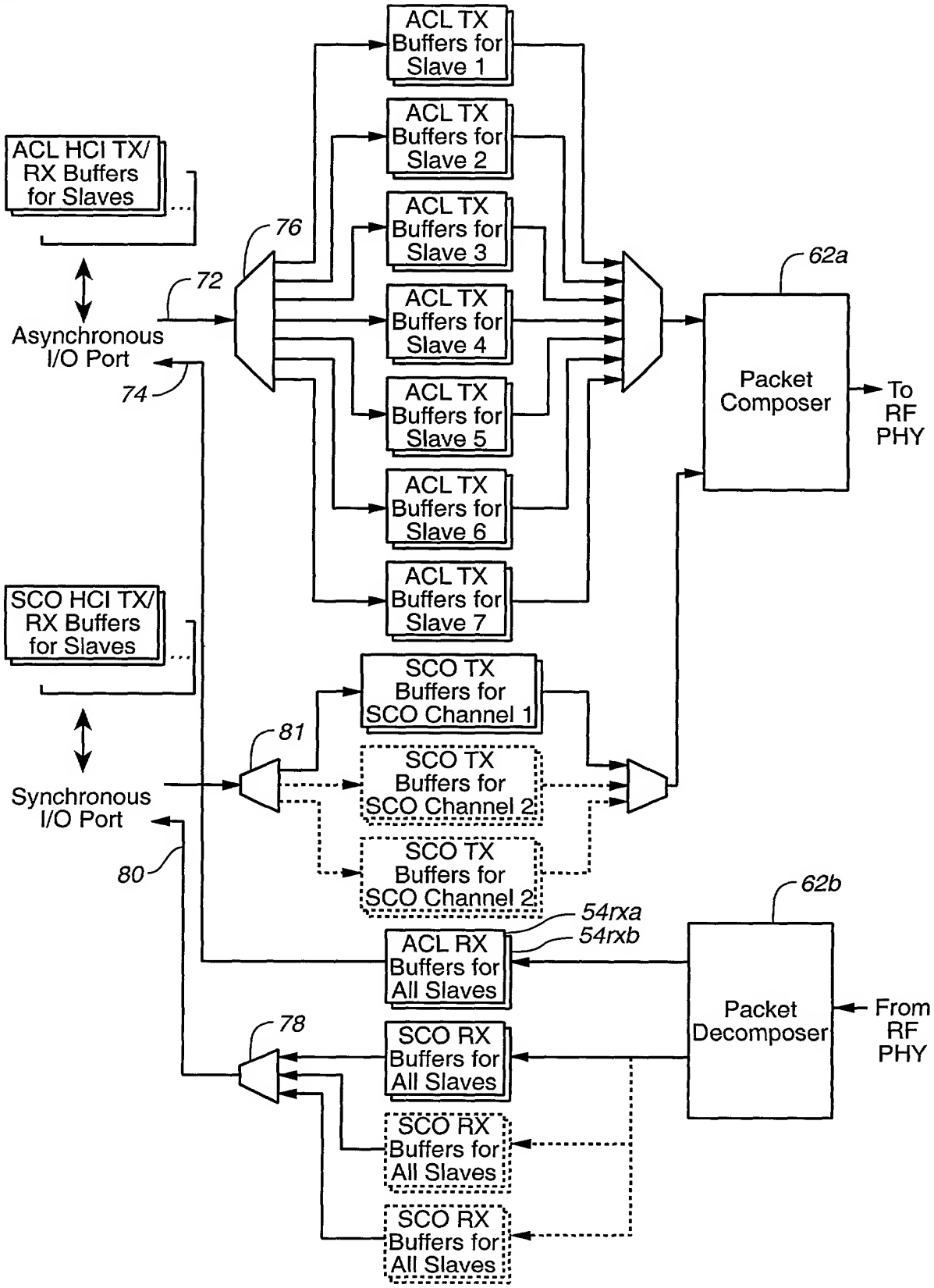


FIG._5B *(PRIOR ART)*

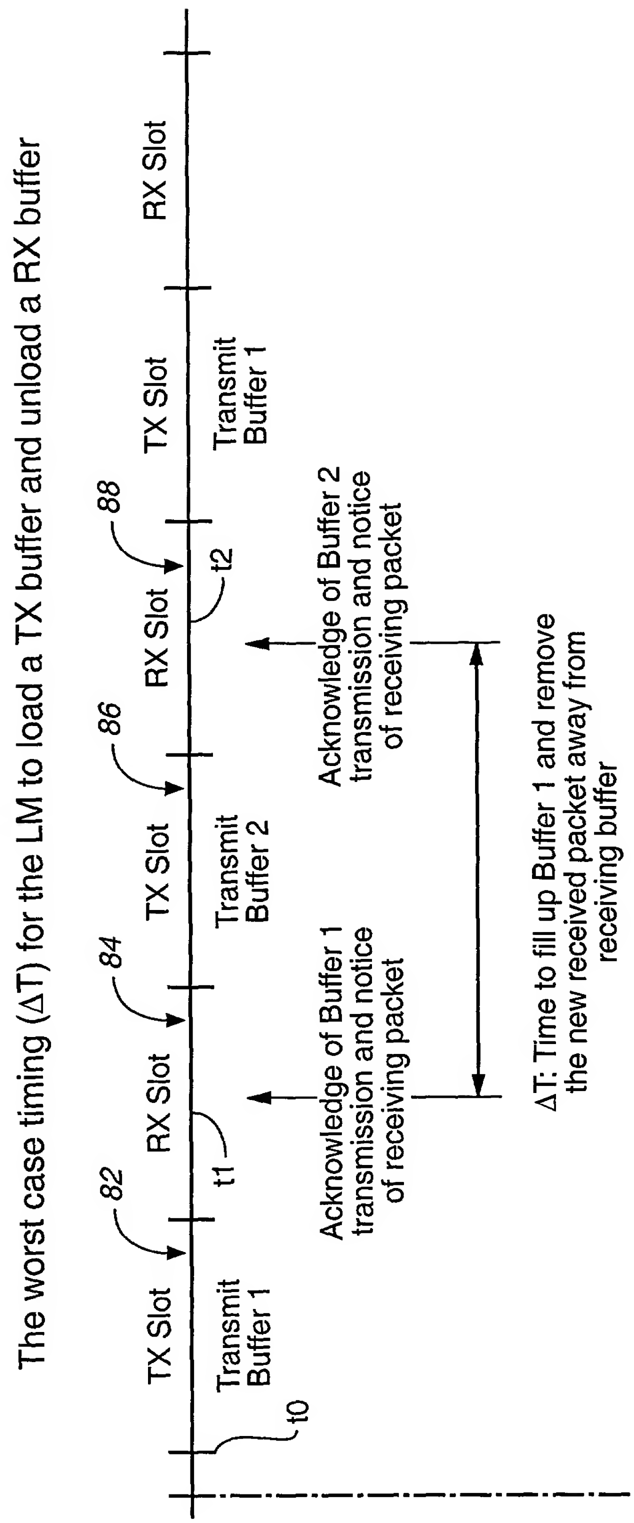


FIG._6
(PRIOR ART)

The Packet Generator accesses the HCI ACL / SCO buffers directly

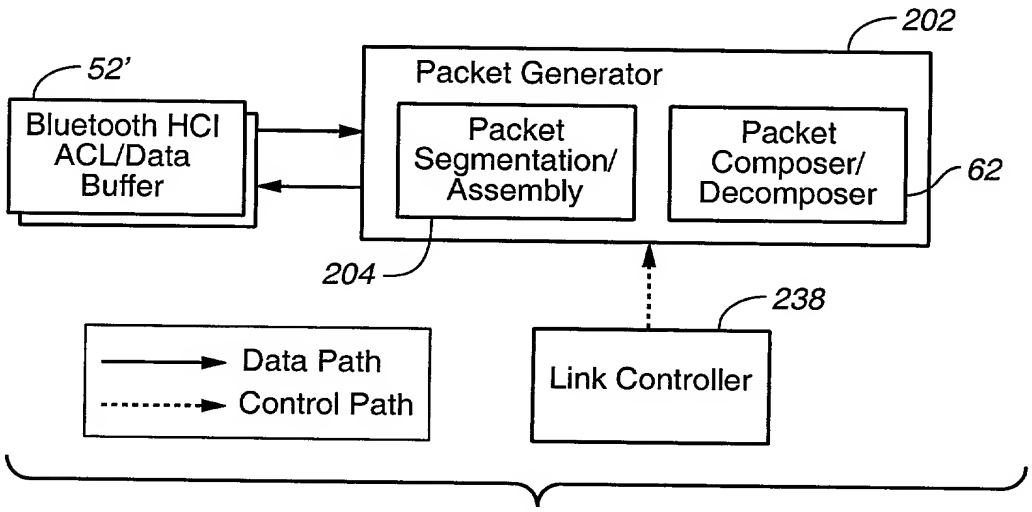


FIG._7

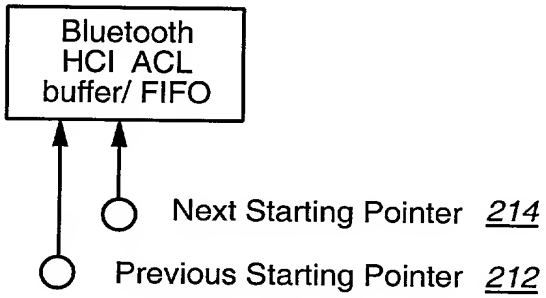


FIG._8

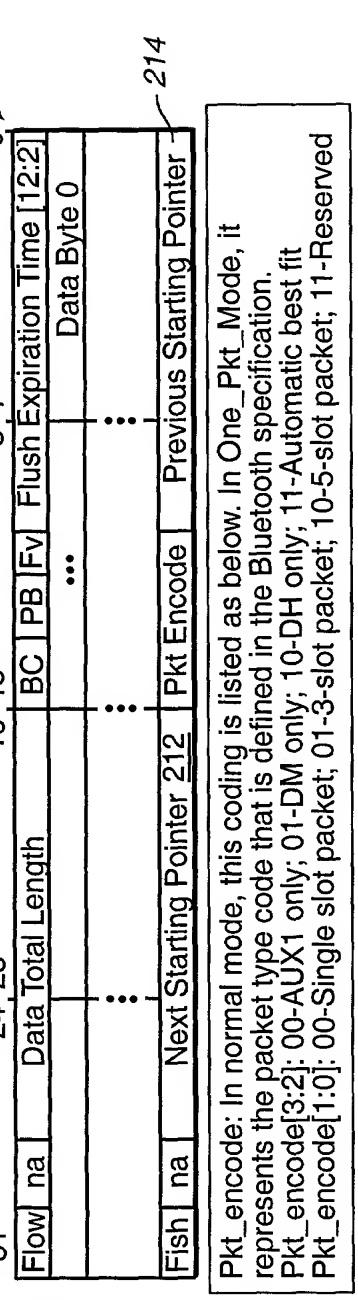


FIG._9A

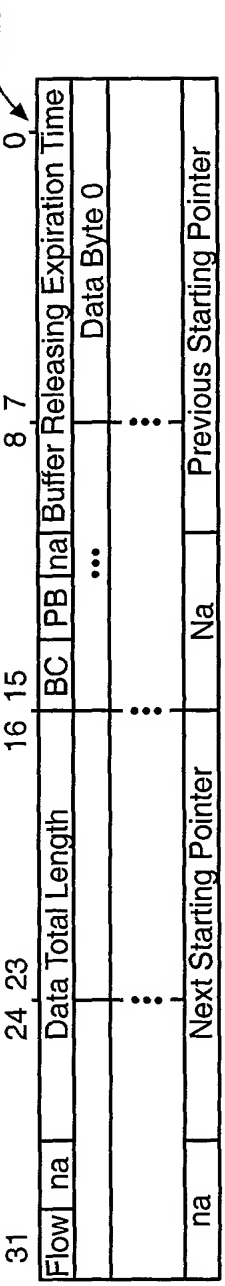


FIG._9B

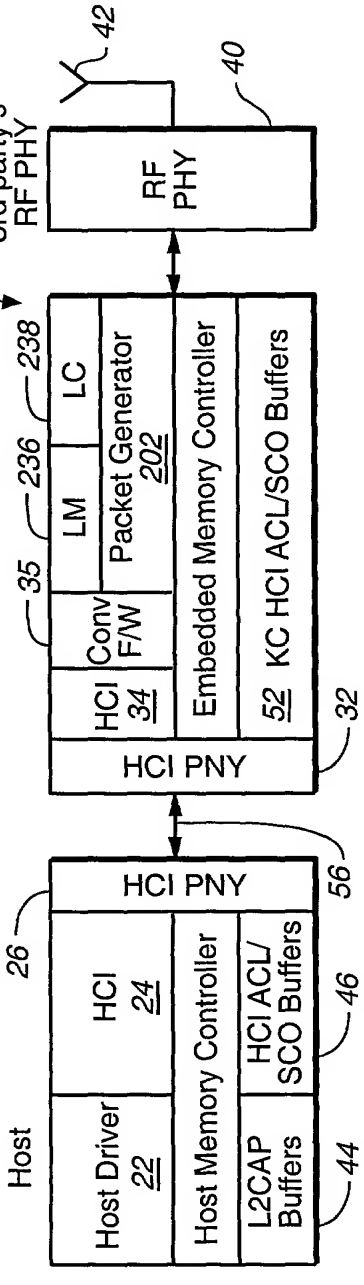


FIG._10

ACL transmission control flow of KC Technology's partition

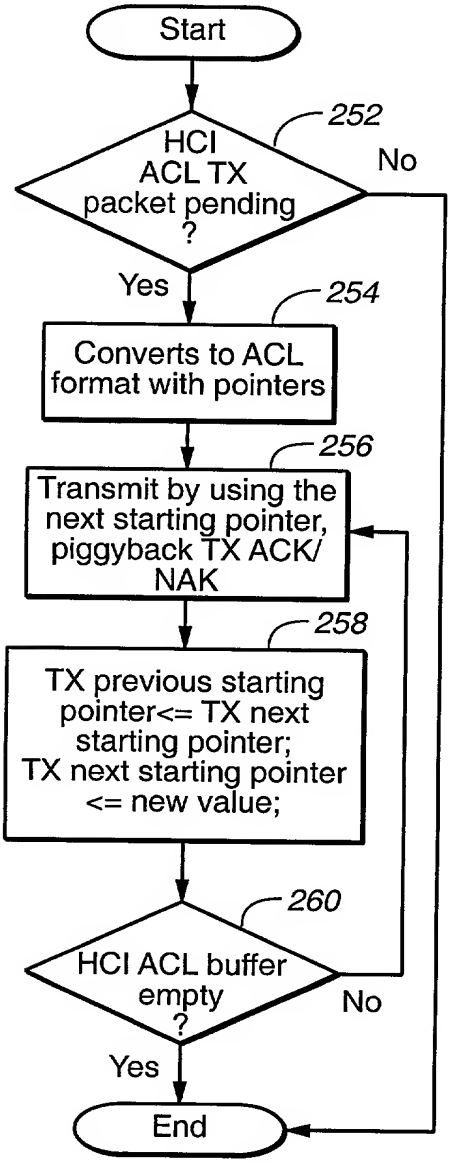


FIG._11

ACL receiving control flow of KC Technology's partition

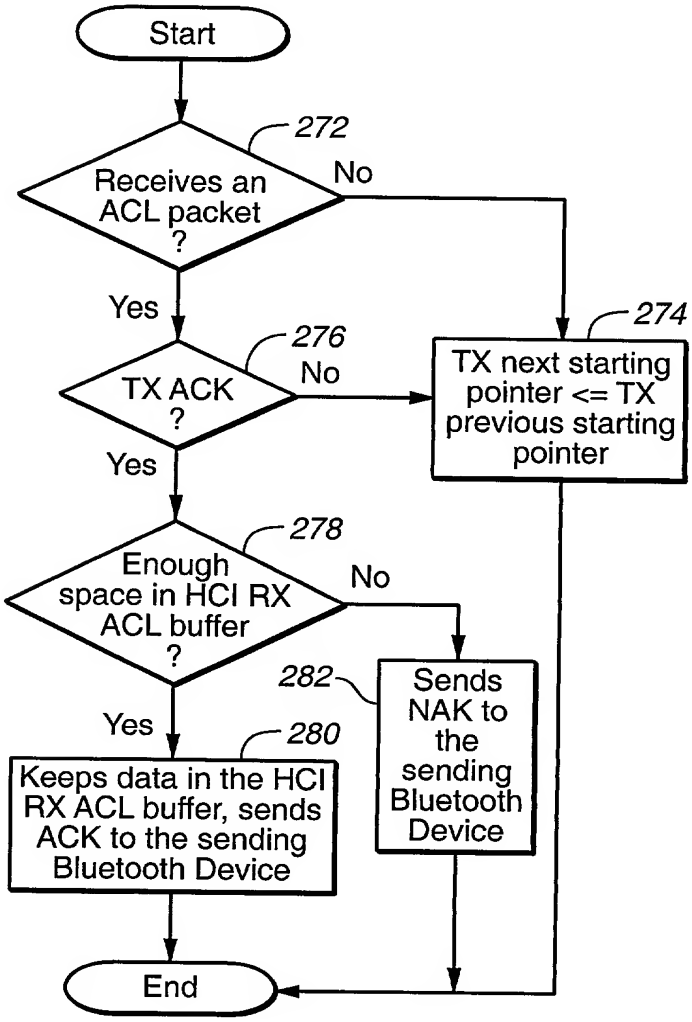


FIG._12

KC Technology's Partition between firmware and hardware

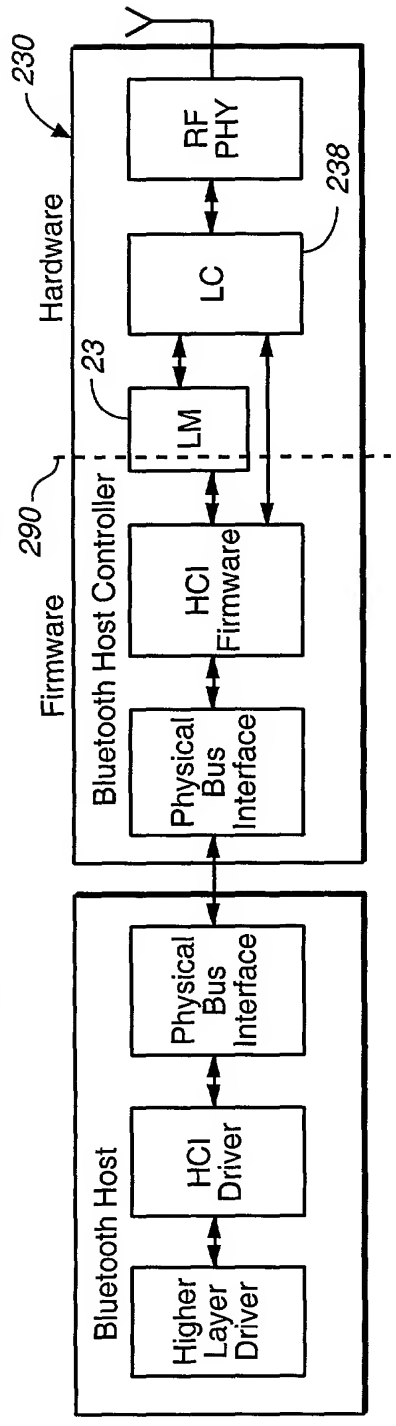


FIG._13

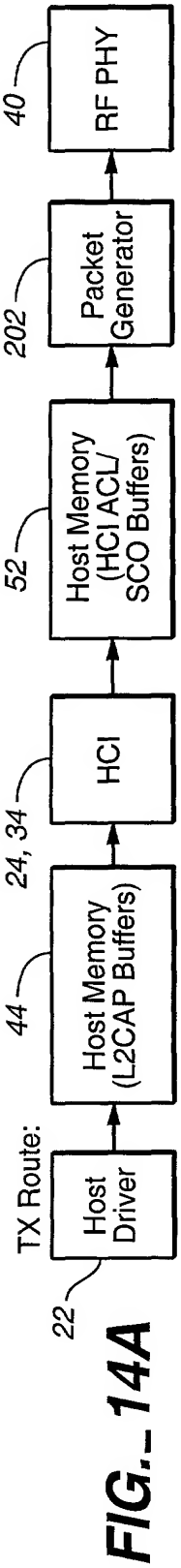


FIG._14A

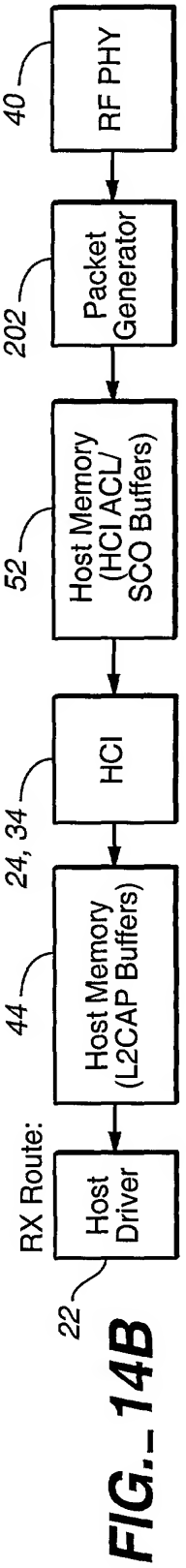


FIG._14B

Type A-2: Host / KC Technology Bluetooth BaseBand Controller

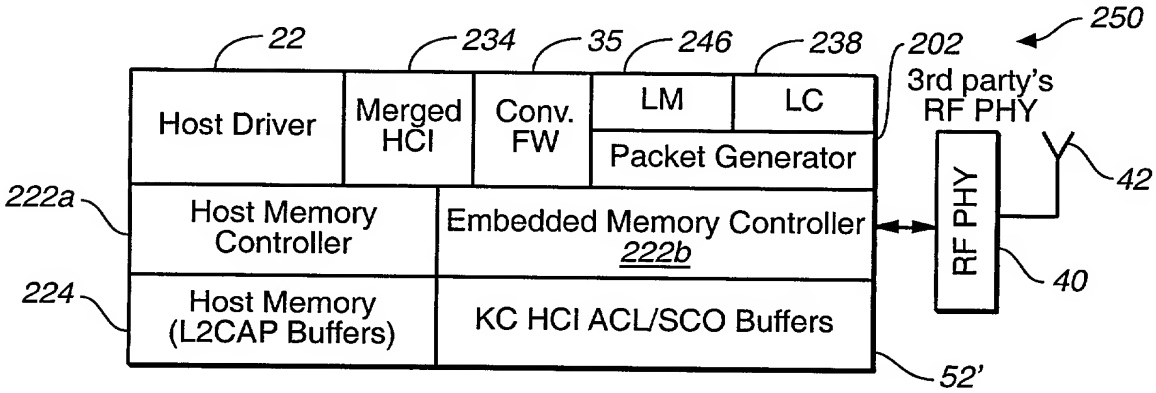


FIG._15A

Type A-2: Host / KC Technology Bluetooth BaseBand Controller

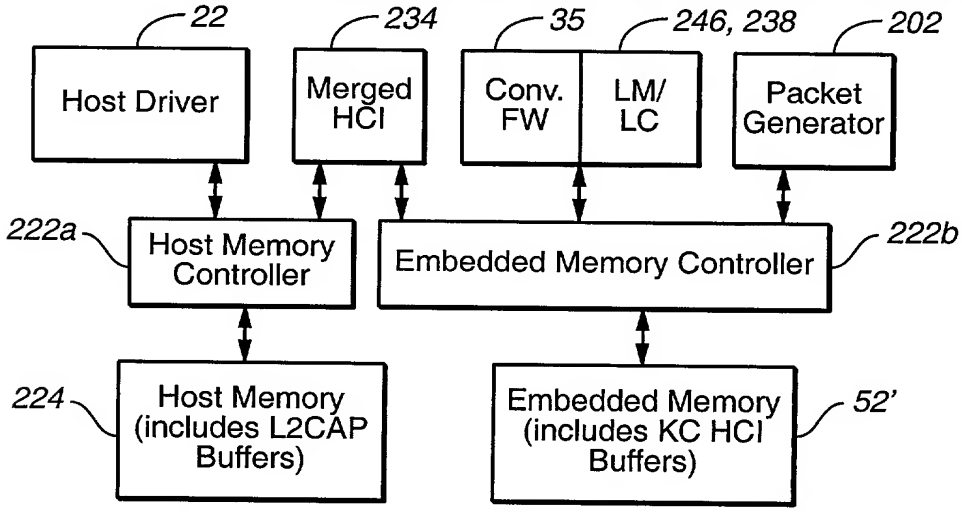


FIG._15B

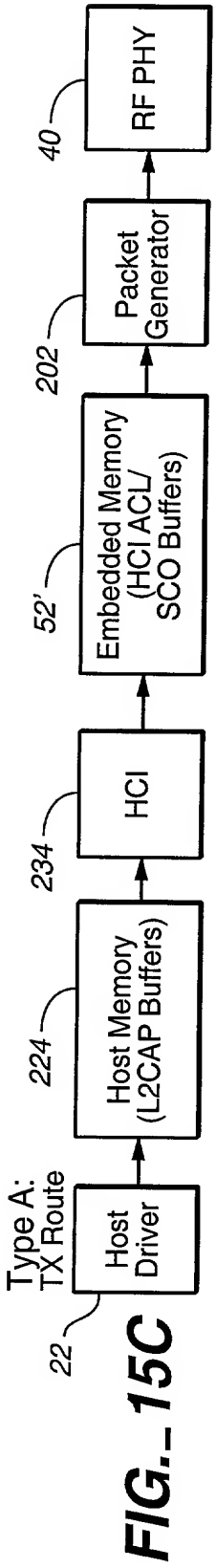


FIG._15C

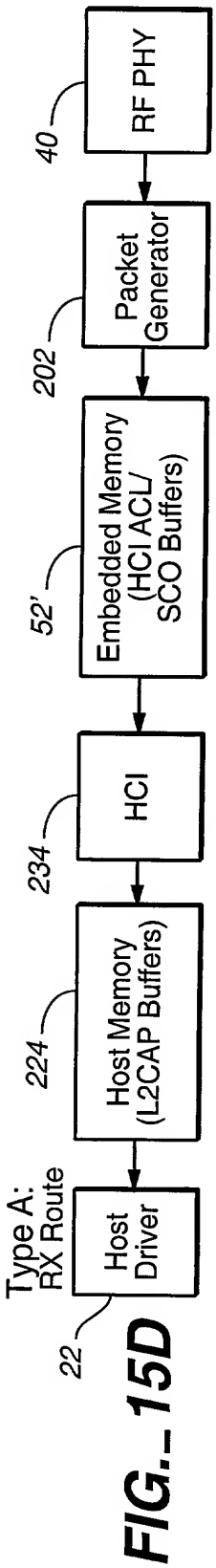


FIG._15D

Type A-1: Host / Bluetooth BaseBand Controller

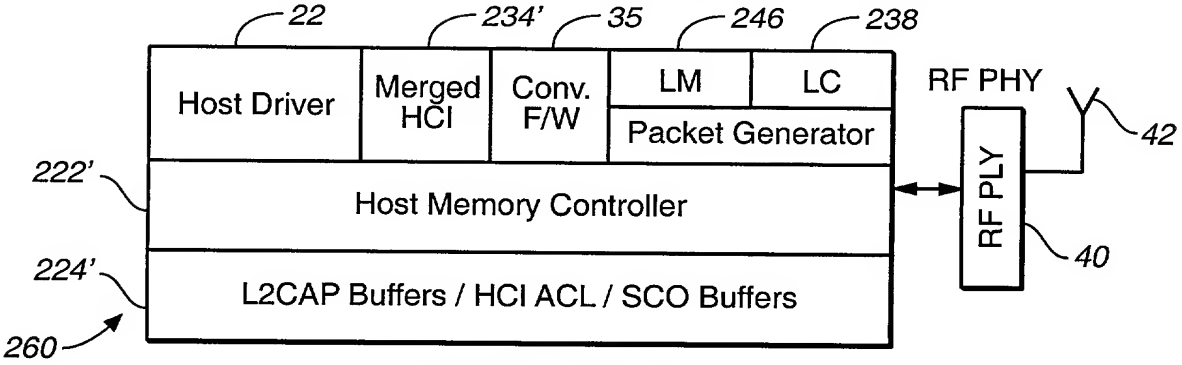


FIG._16A

TYPE A-1: Host / Bluetooth BaseBand Controller

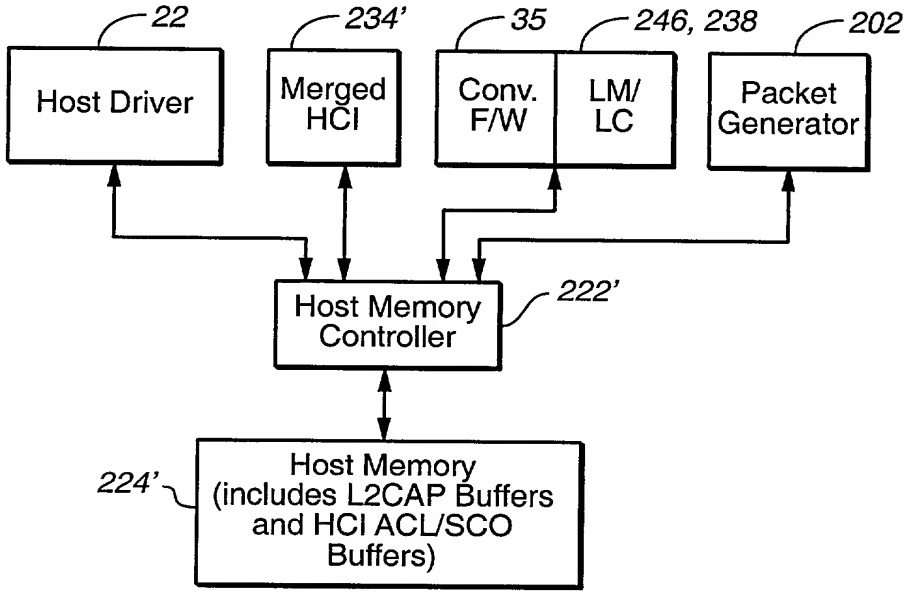


FIG._16B

Type B: Host / Bluetooth BaseBand Controller

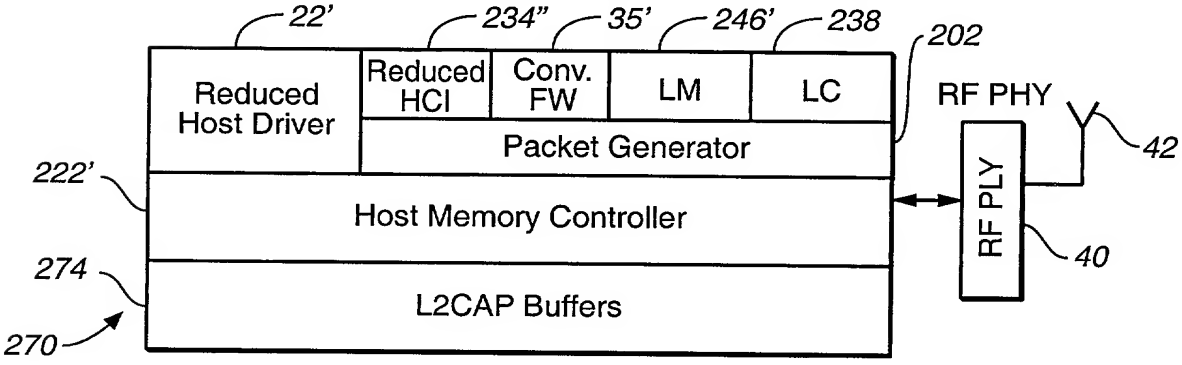


FIG._17A

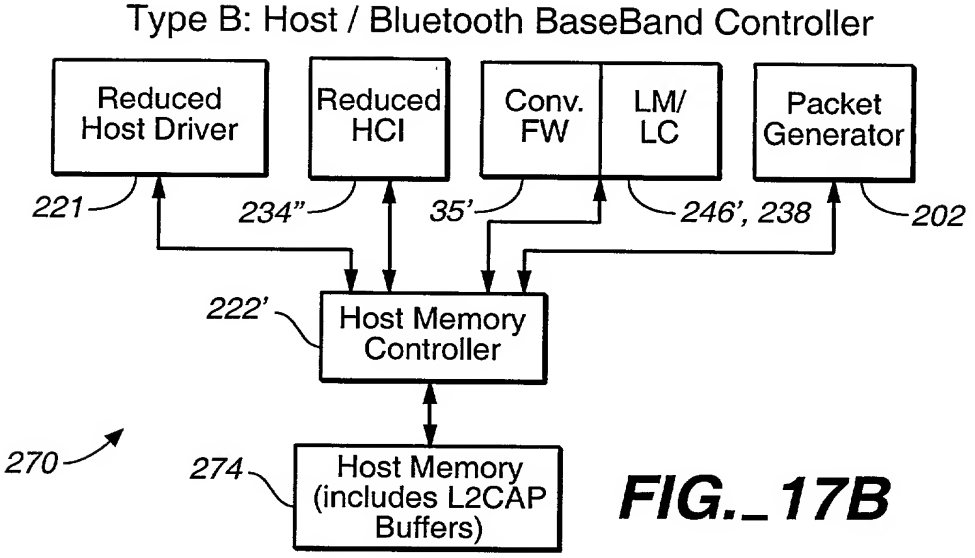


FIG._17B

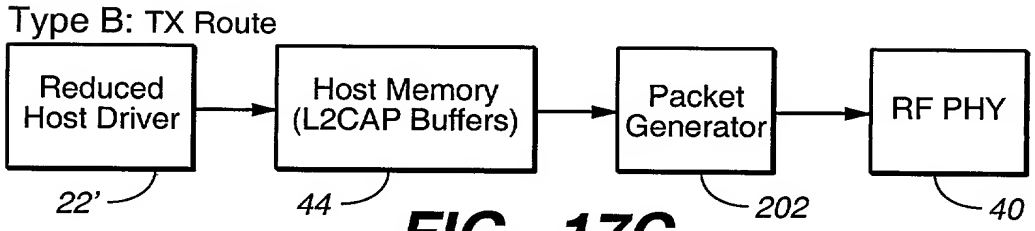


FIG._17C

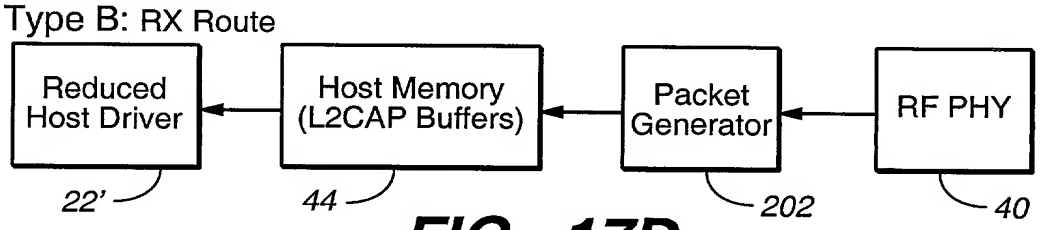


FIG._17D

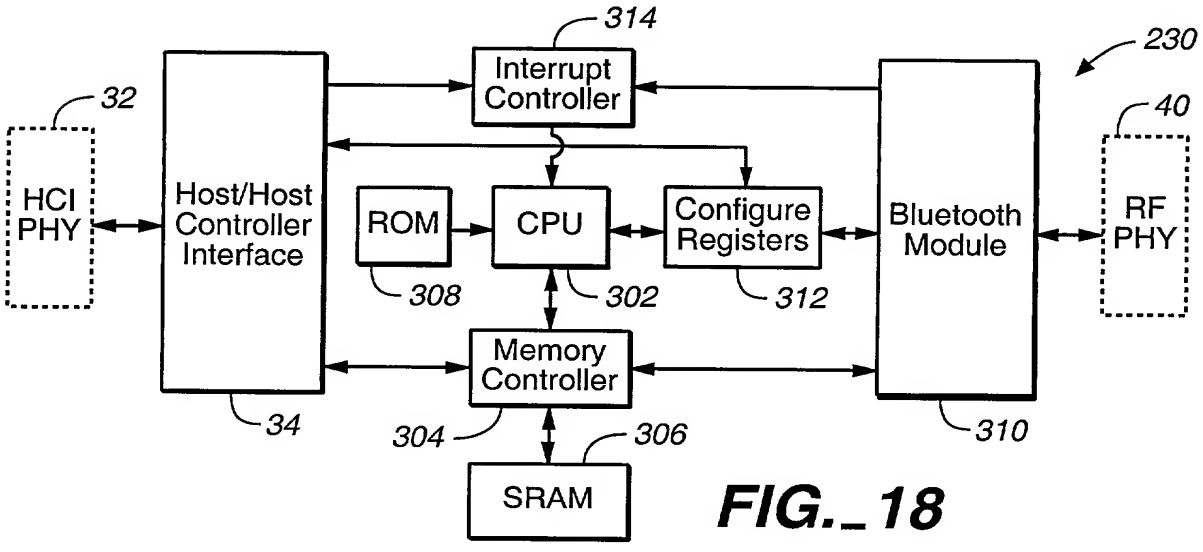
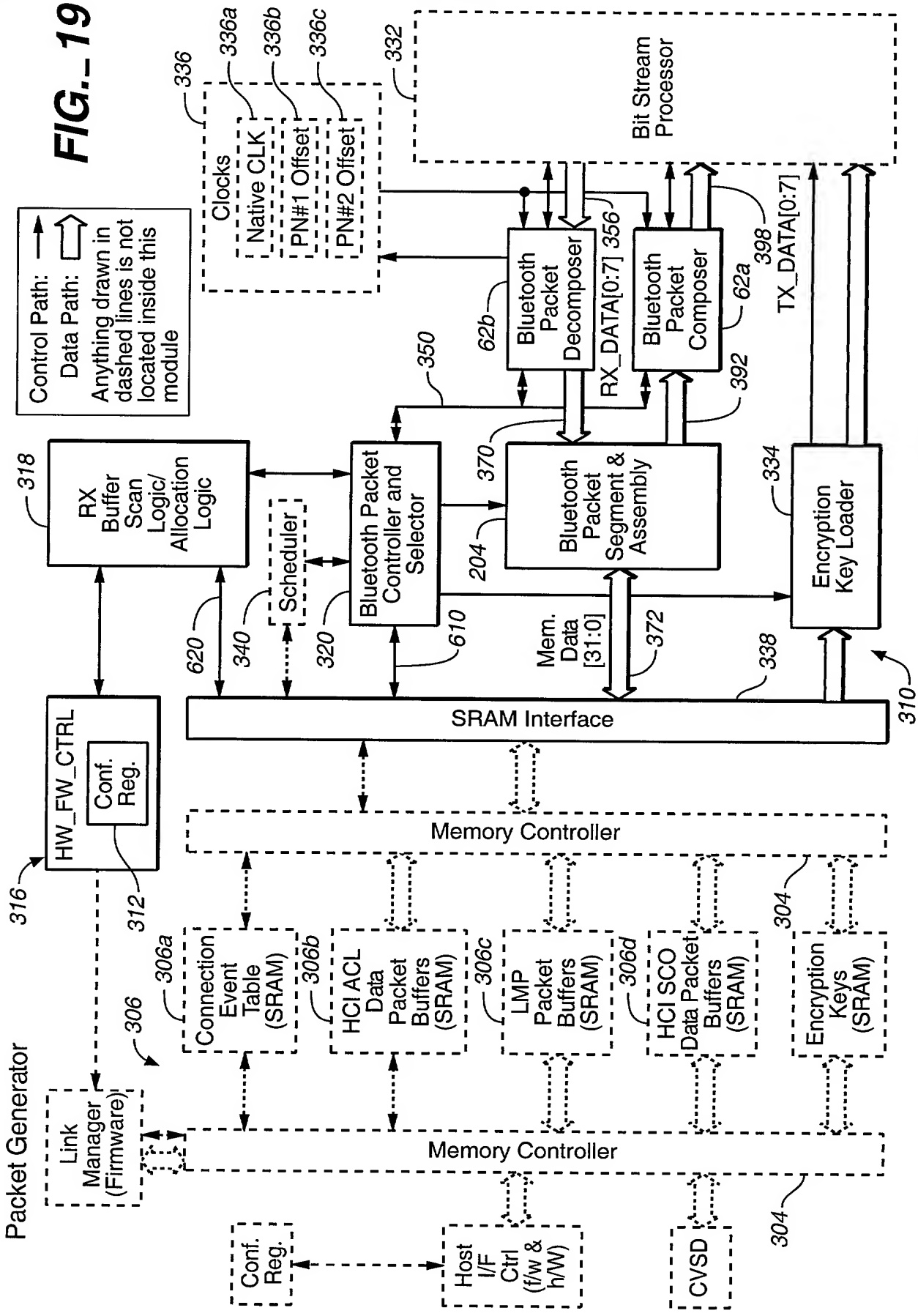


FIG._18

FIG._19



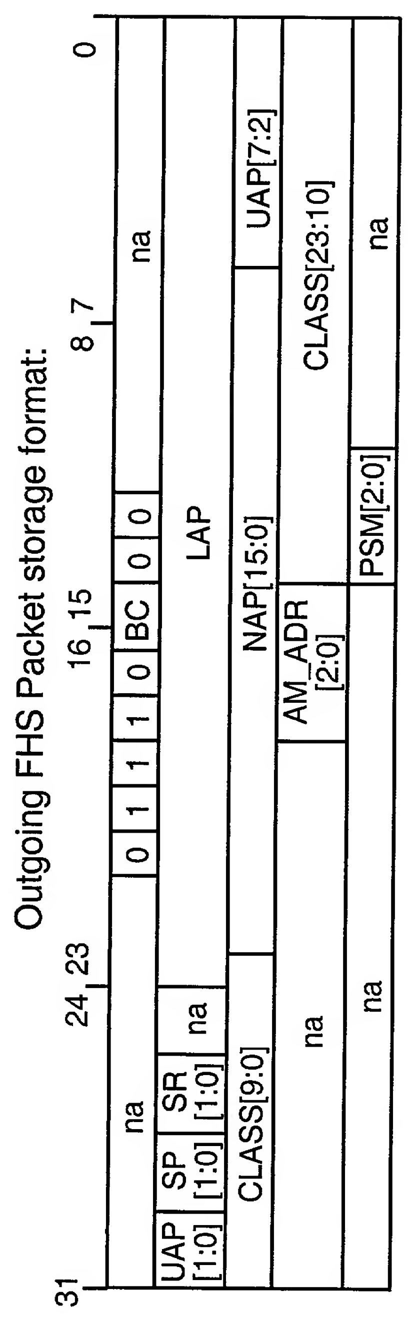


FIG._20

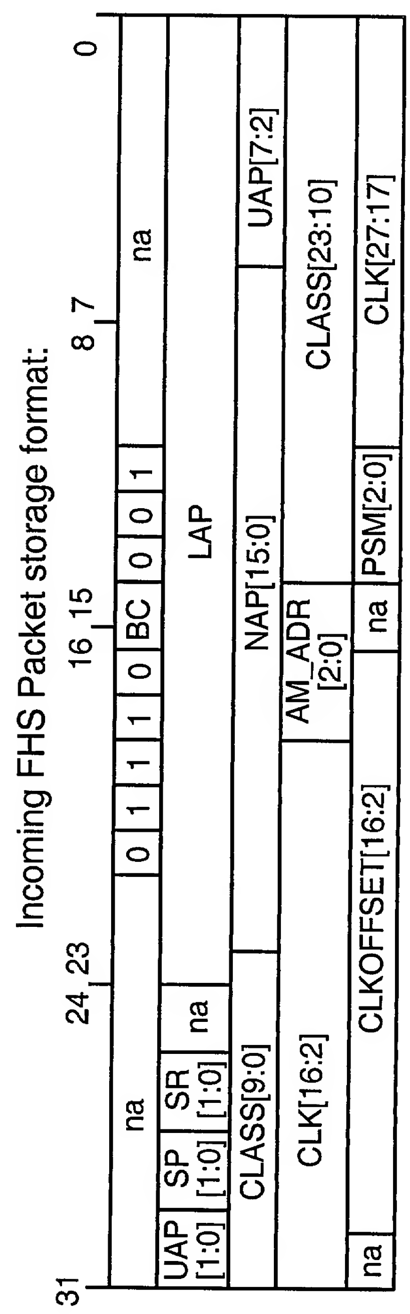


FIG._21

Data Byte Sending Sequence in FHS packet:

Byte# & name	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7
1:Packet Header 0	amadr0	amadr2	amadr2	pkttp0	pkttp1	pkttp2	pkttp3	flow
2:Packet Header 1	arqn	seqn	–	–	–	–	–	–
3:FHS 0	lap0	lap1	lap2	lap3	lap4	lap5	lap6	lap7
4:FHS 1	lap8	lap9	lap10	lap11	lap12	lap13	lap14	lap15
5:FHS 2	lap16	lap17	lap18	lap19	lap20	lap21	lap22	lap23
6:FHS 3	tbd0	tbd1	sr0	sr1	sp0	sp1	uap0	uap1
7:FHS 4	uap2	uap3	uap4	uap5	uap6	uap7	nap0	nap1
8:FHS 5	nap2	nap3	nap4	nap5	nap6	nap7	nap8	nap9
9:FHS 6	nap10	nap11	nap12	nap13	nap14	nap15	clss0	clss1
10:FHS 7	clss2	clss3	clss4	clss5	clss6	clss7	clss8	clss9
11:FHS 8	clss10	clss11	clss12	clss13	clss14	clss15	clss16	clss17
12:FHS 9	clss18	clss19	clss20	clss21	clss22	clss23	amad0	amad1
13:FHS 10	amad2							
14:FHS 11								
15:FHS 12								
16:FHS 13				pgscn0	pgscn1	pgscn2	–	–

FIG._22

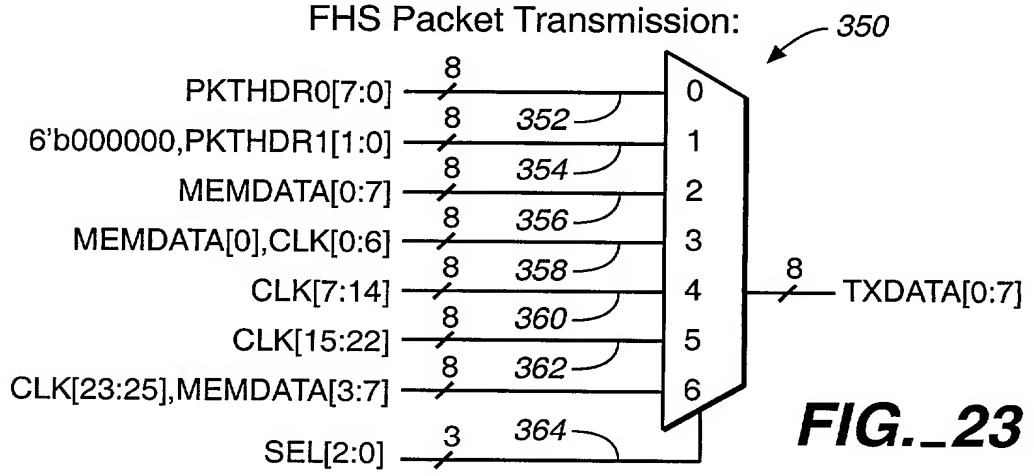


FIG._23

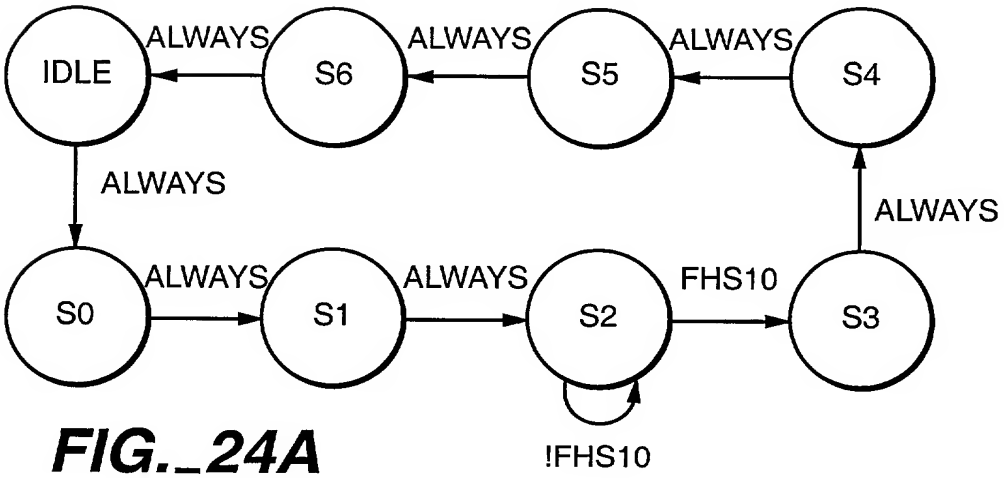


FIG._24A

FIG._24B

State	SEL[2:0]
IDLE	0
S0	0
S1	1
S2	2
S3	3
S4	4
S5	5
S6	6

Data Byte Sending Sequence in DM1 packet:

Byte# & name	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7
1:Packet Header 0	amadr0	amadr1	amadr2	pkttp0	pkttp1	pkttp2	pkttp3	flow
2:Packet Header 1	arqn	seqn	–	–	–	–	–	–
3:Payload Header 0	l_ch 0	l_ch 1	pld_flow	length0	length1	length2	length3	length4
4:ACL data 1	data bit 0	data bit 1	data bit 2	data bit 3	data bit 4	data bit 5	data bit 6	data bit 7
5:ACL data 2	data bit 0	data bit 1	data bit 2	data bit 3	data bit 4	data bit 5	data bit 6	data bit 7
...	...	...	...	...	...	...	...	...
n+3:ACL data n	data bit 0	data bit 1	data bit 2	data bit 3	data bit 4	data bit 5	data bit 6	data bit 7

n: data length

FIG._25

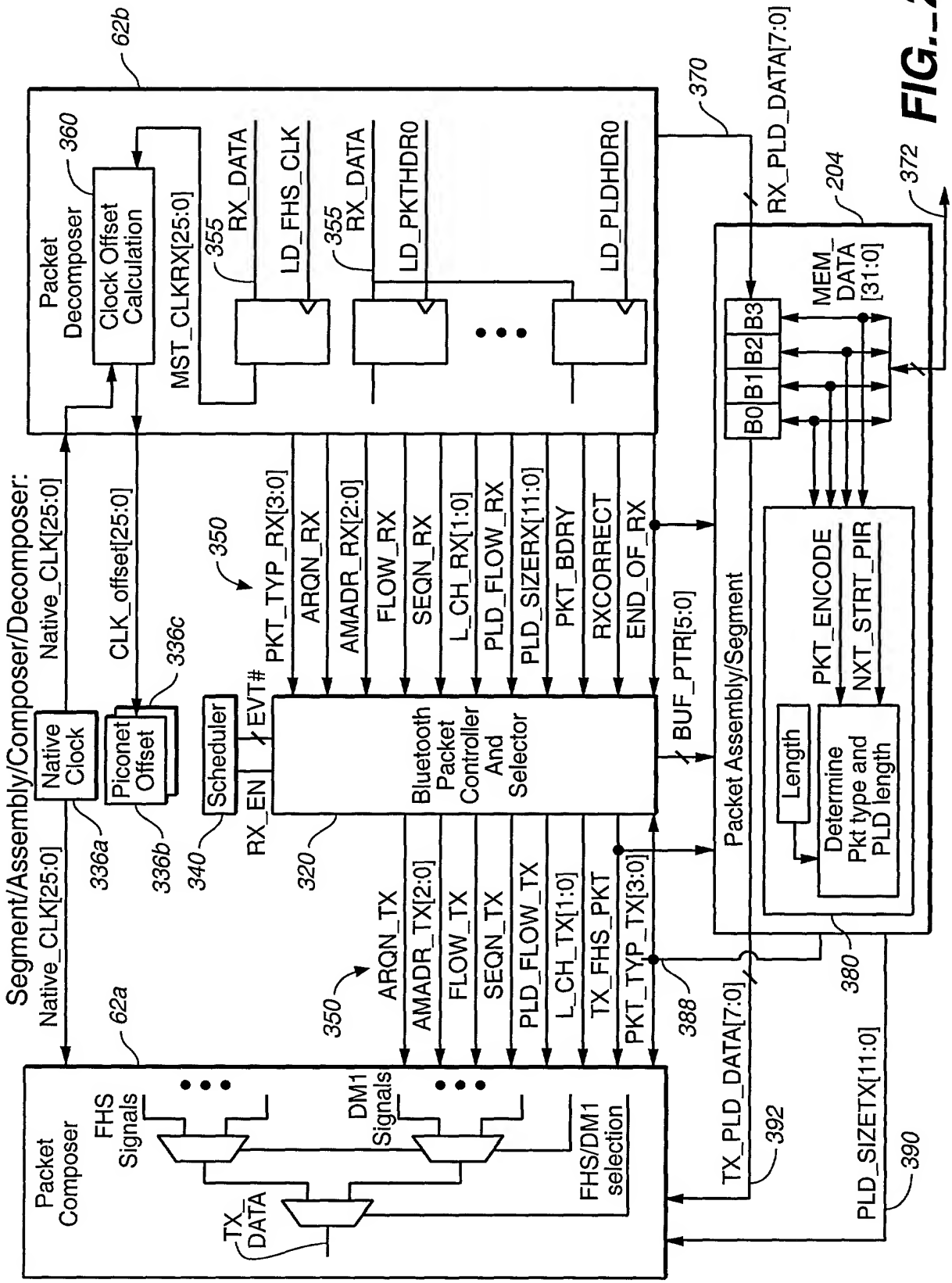


FIG._26

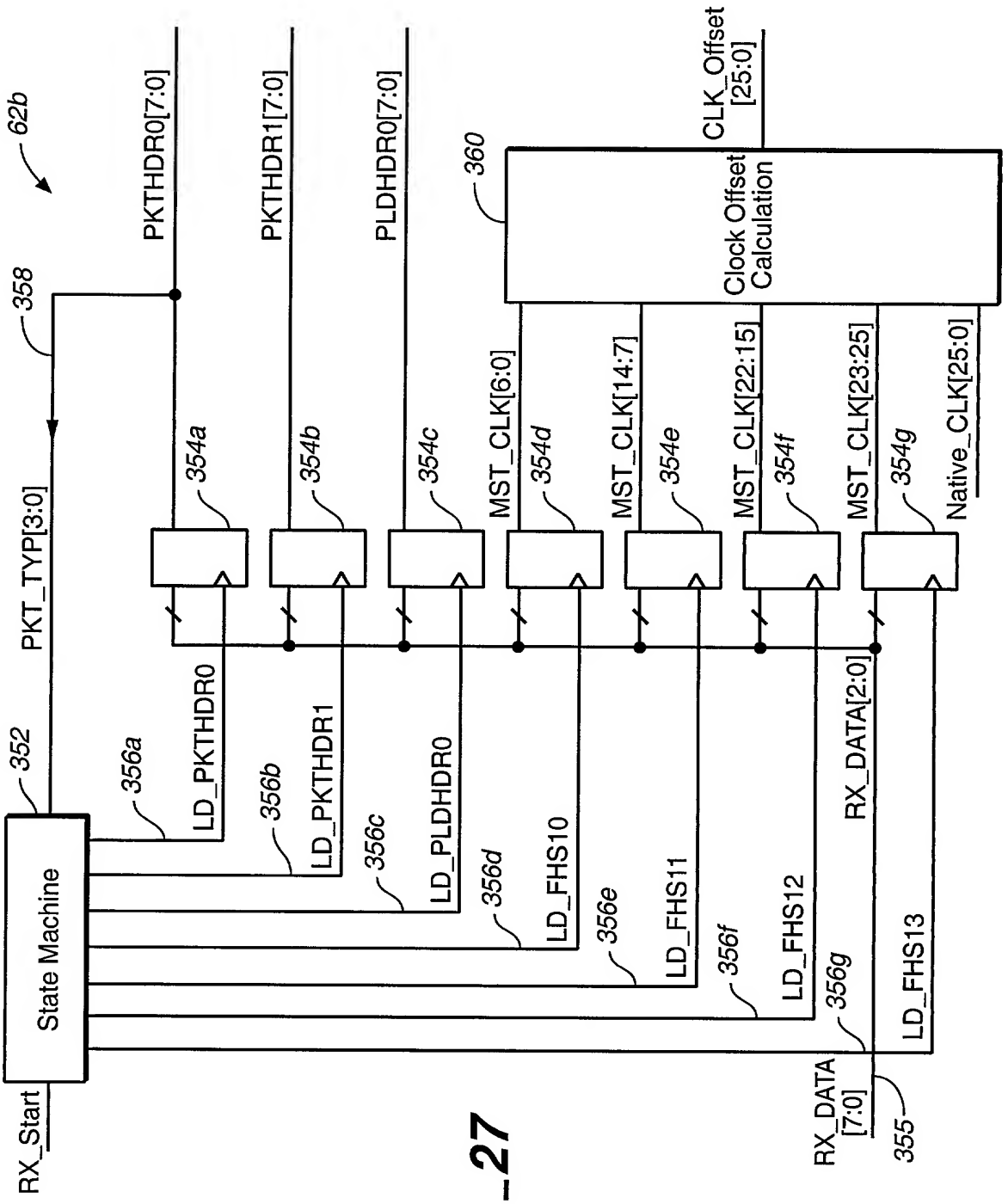


FIG._27

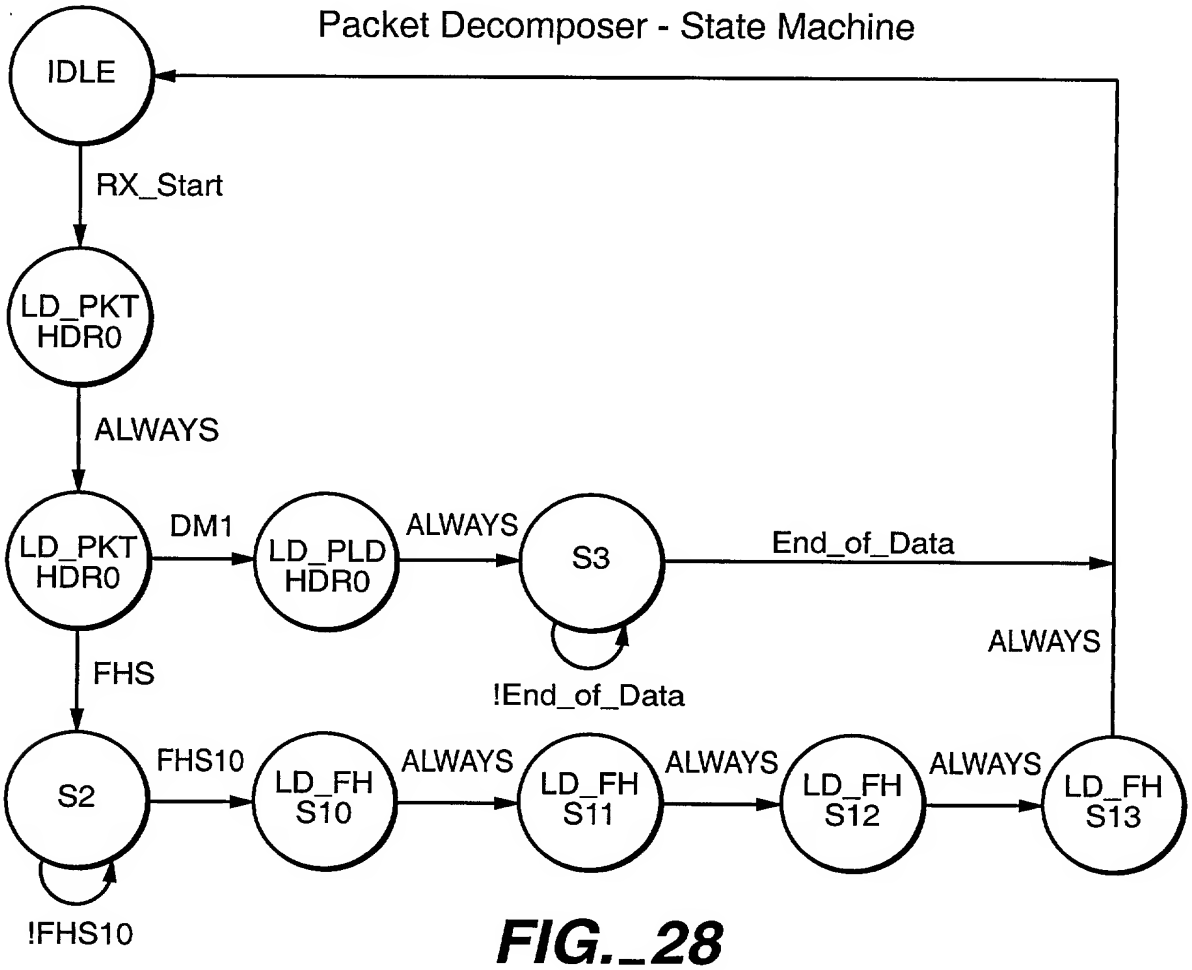


FIG._28

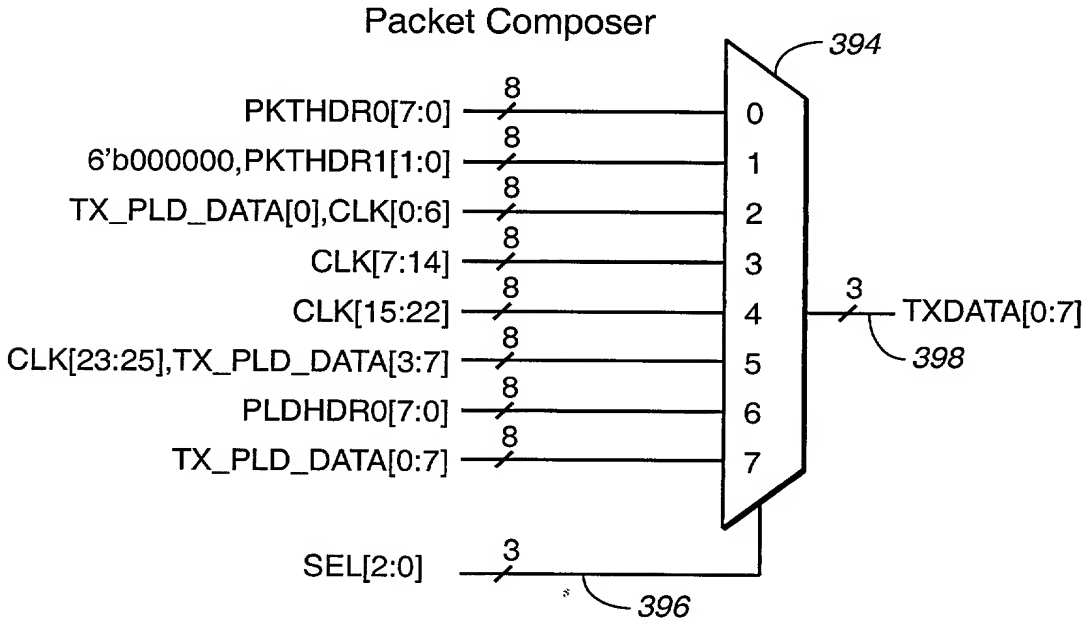


FIG._30

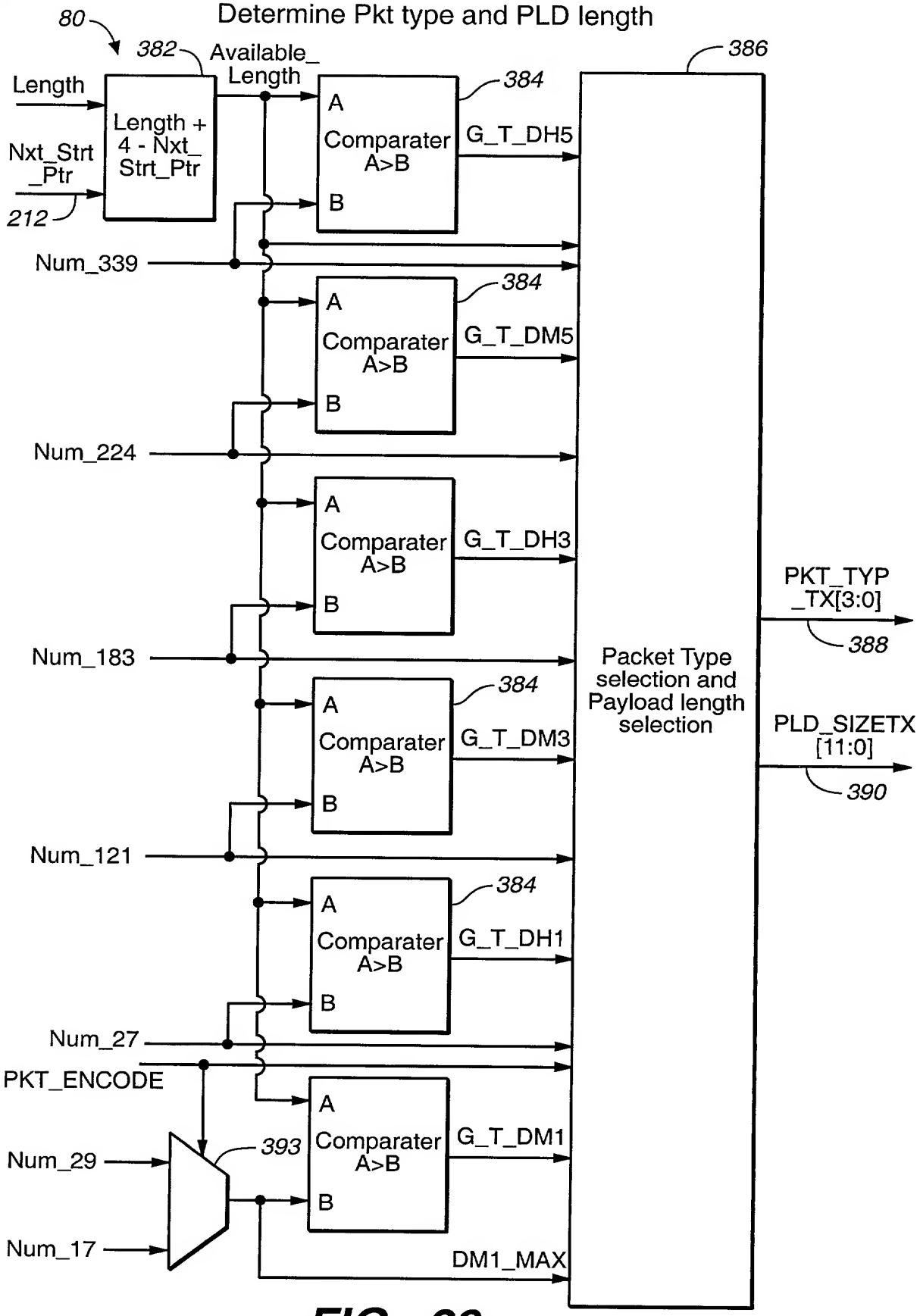


FIG._29

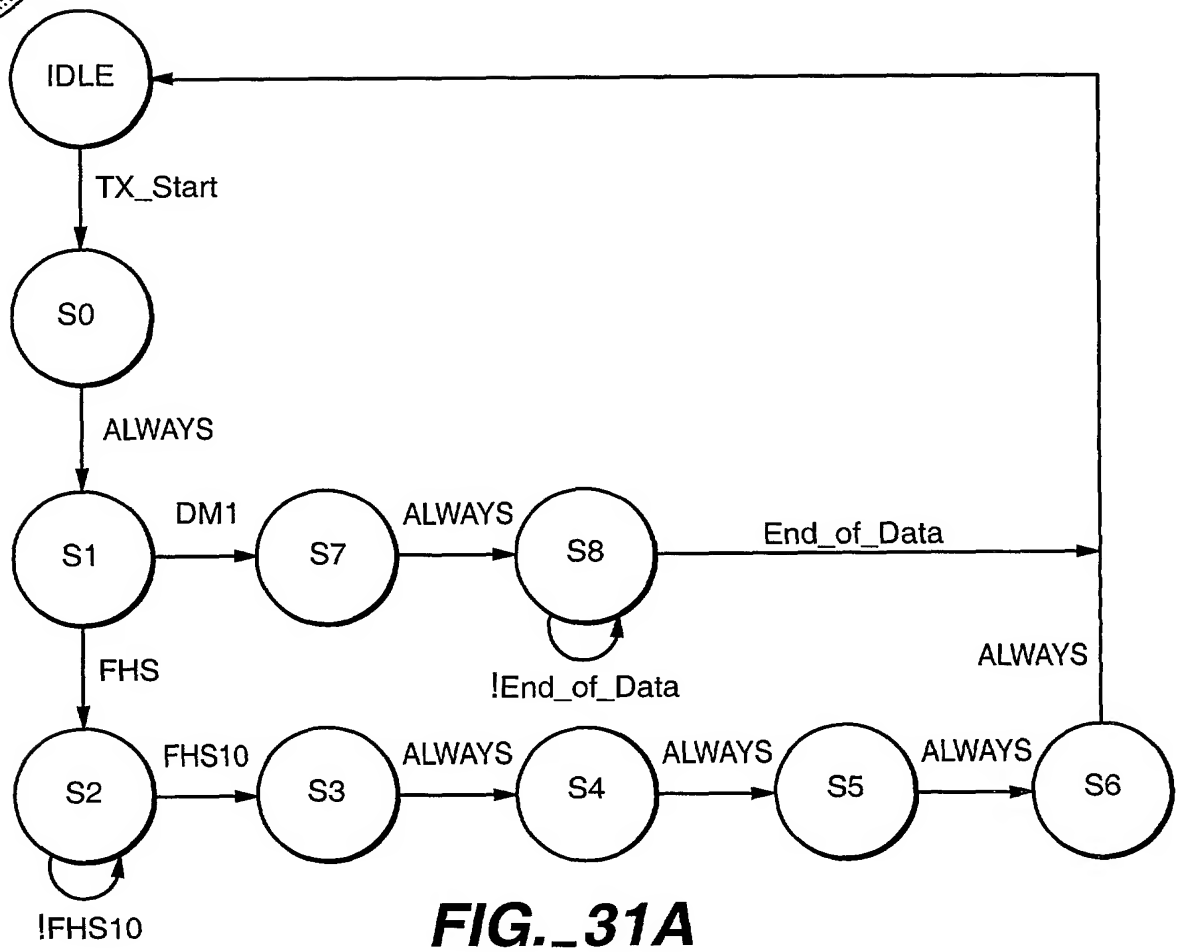


FIG._31A

State	SEL[2:0]
IDLE	0
S0	0
S1	1
S2	7
S3	2
S4	3
S5	4
S6	5
S7	6
S8	7

FIG._31B

Dual pointer buffer control scheme (1)

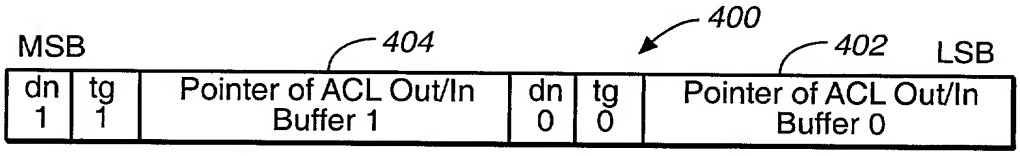


FIG._32

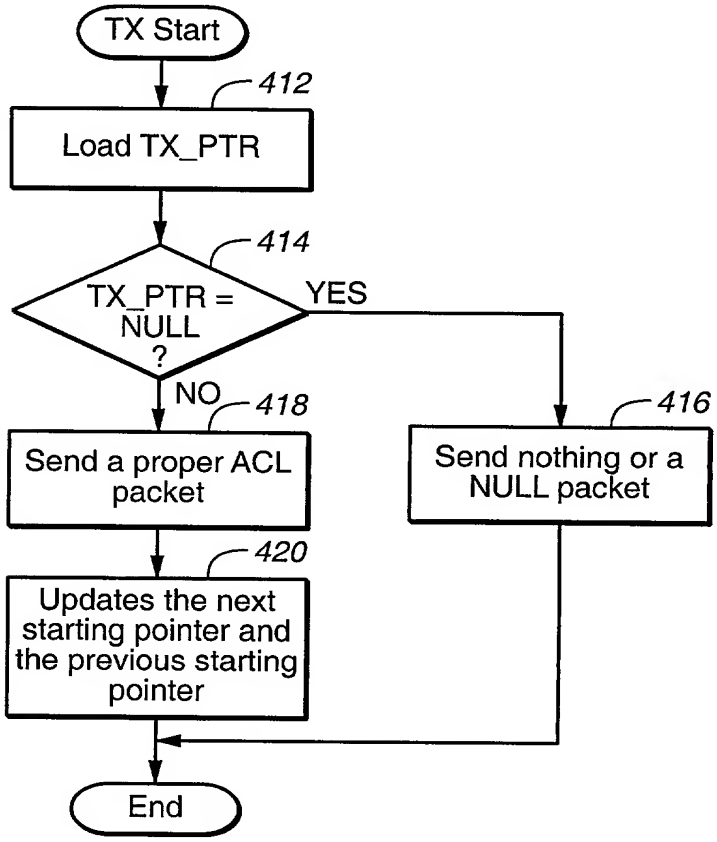


FIG._33

How to convert between the L2CAP packet format and buffer format

L2CAP Packet Format

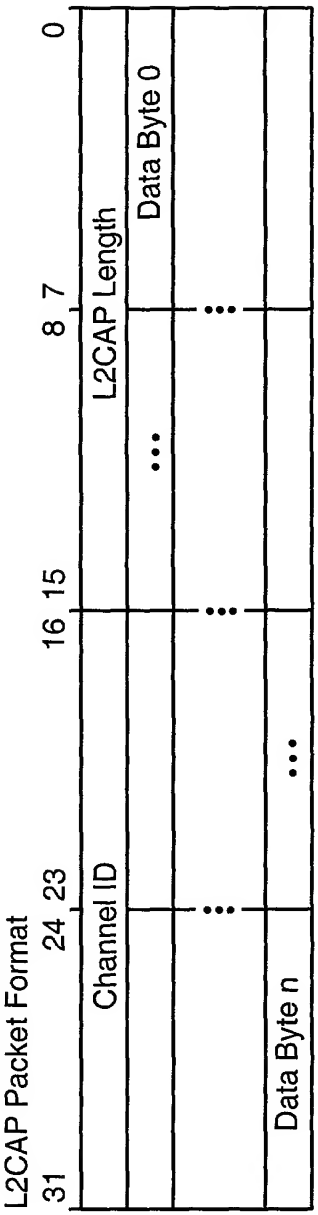


FIG._34A

How to convert between the L2CAP packet format and buffer format

ACL Buffer while Sending

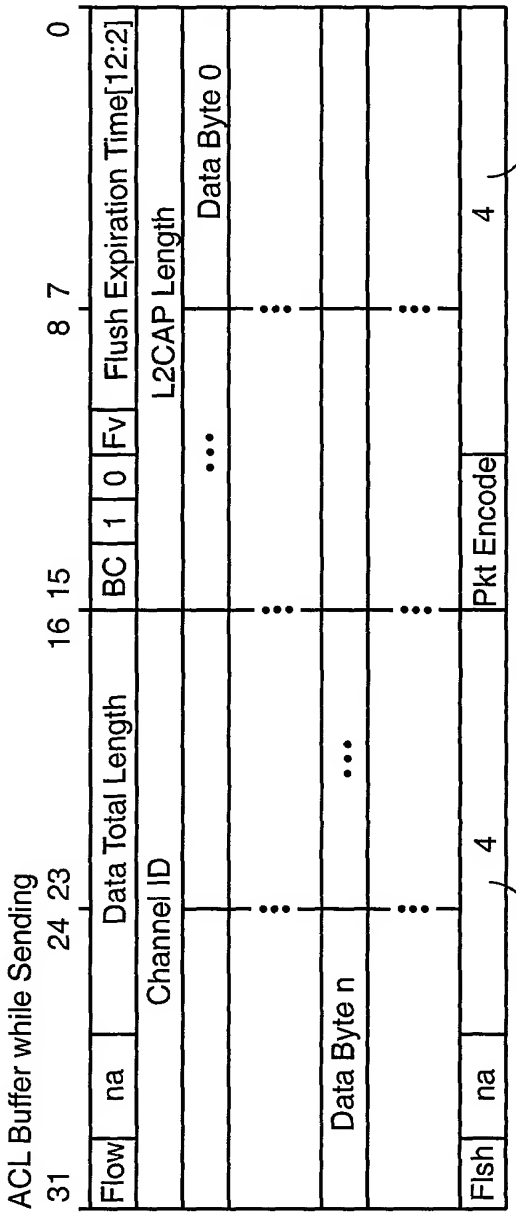


FIG._34B

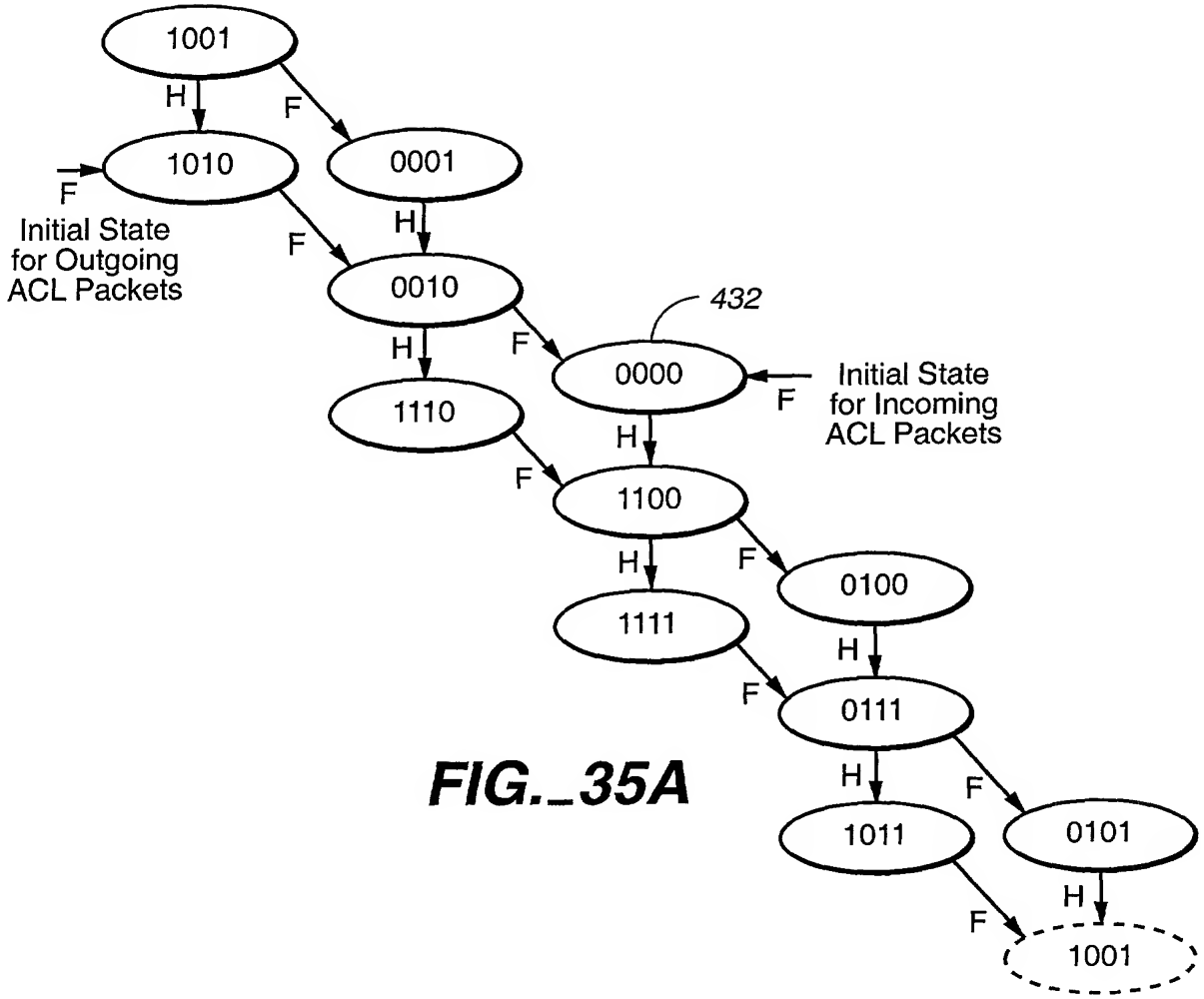


FIG._35A

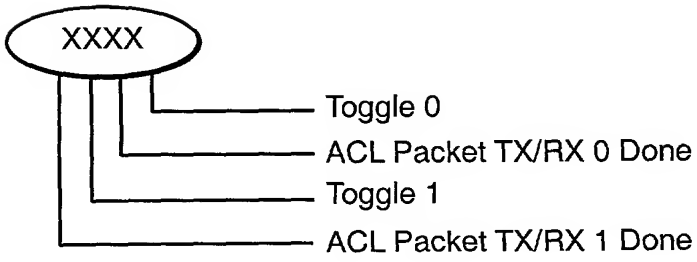


FIG._35B

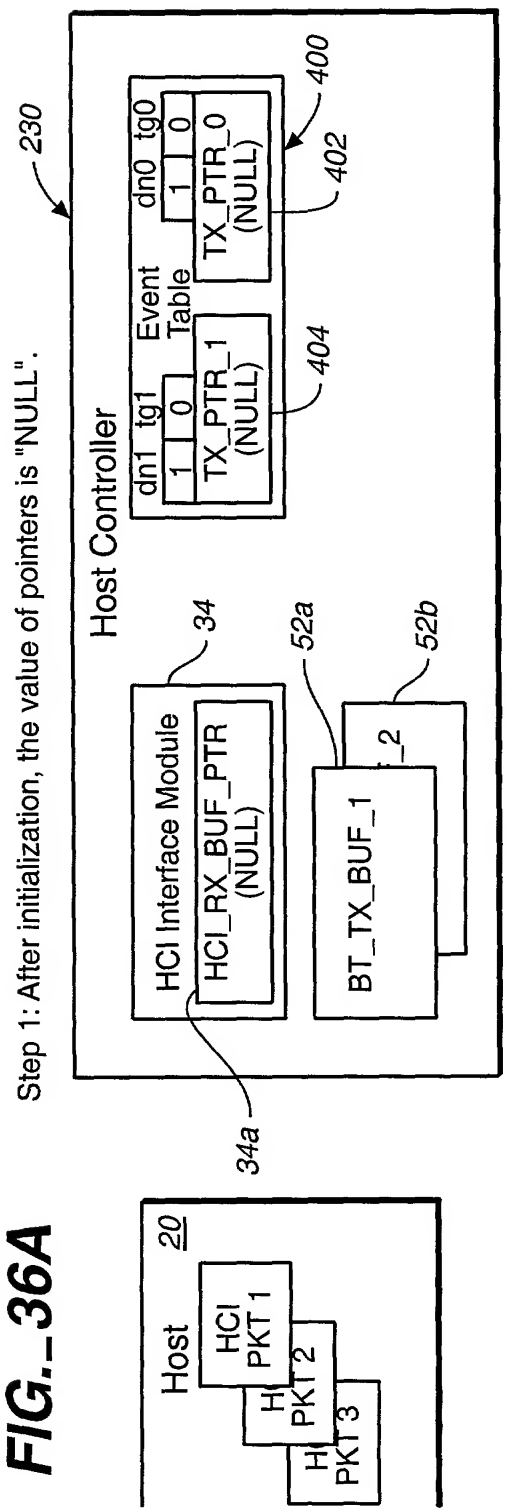


FIG._36A

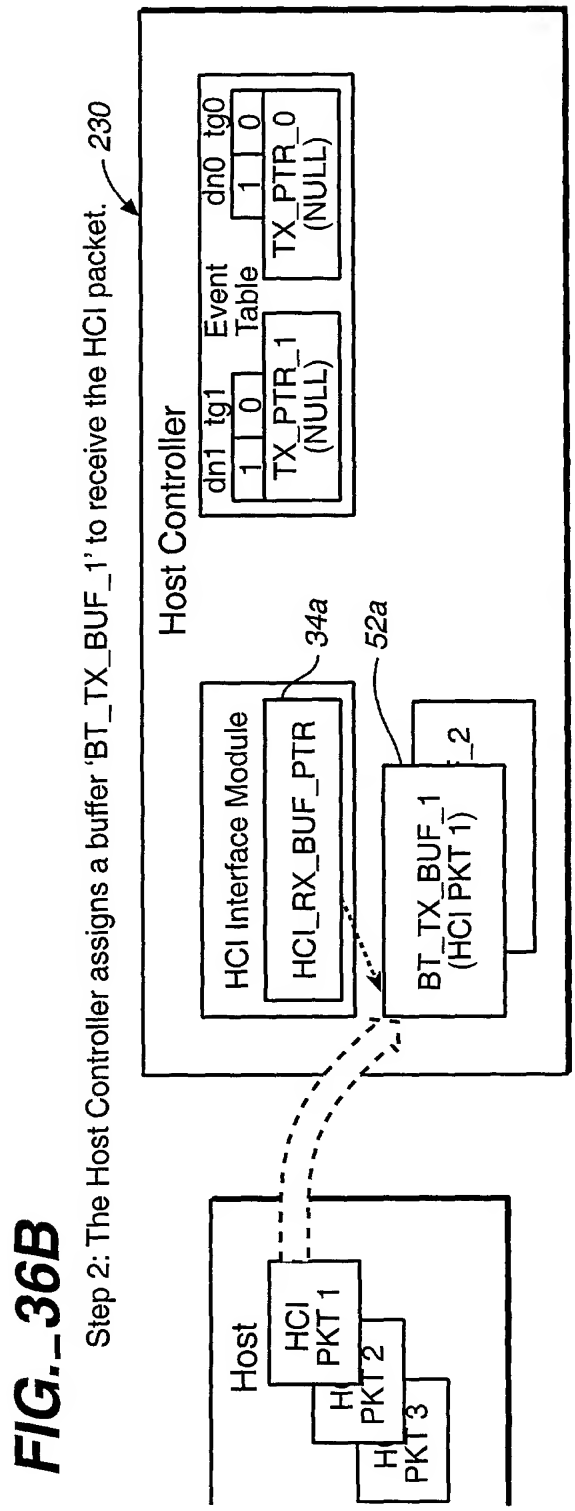


FIG._36B

FIG._36C

Step 3: The HCI packet 'HCI PKT 1' is stored in the buffer 'BT_TX_BUF_1'.

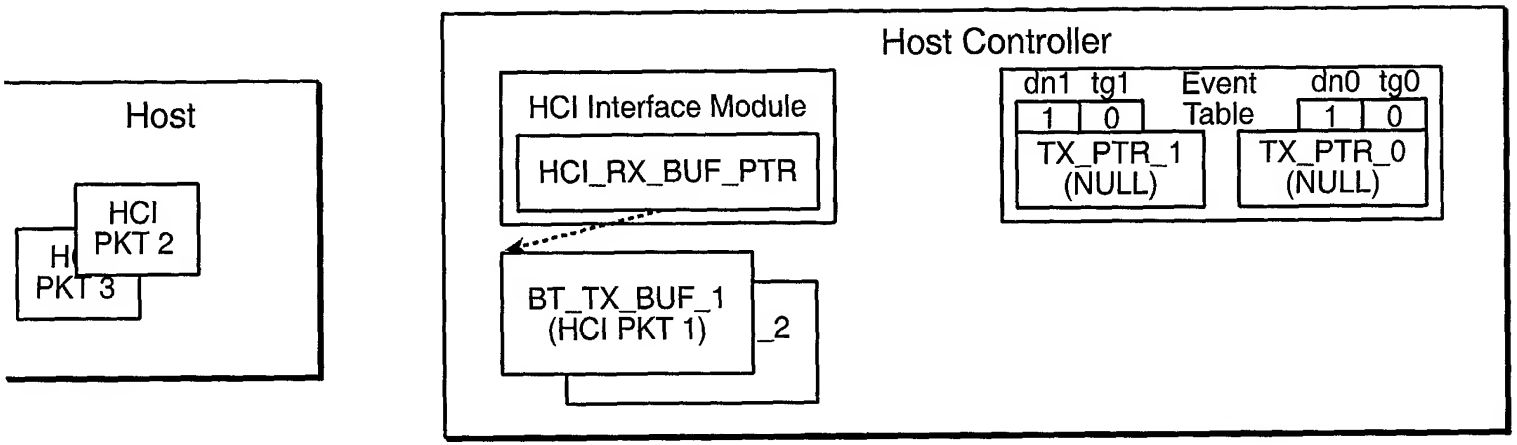
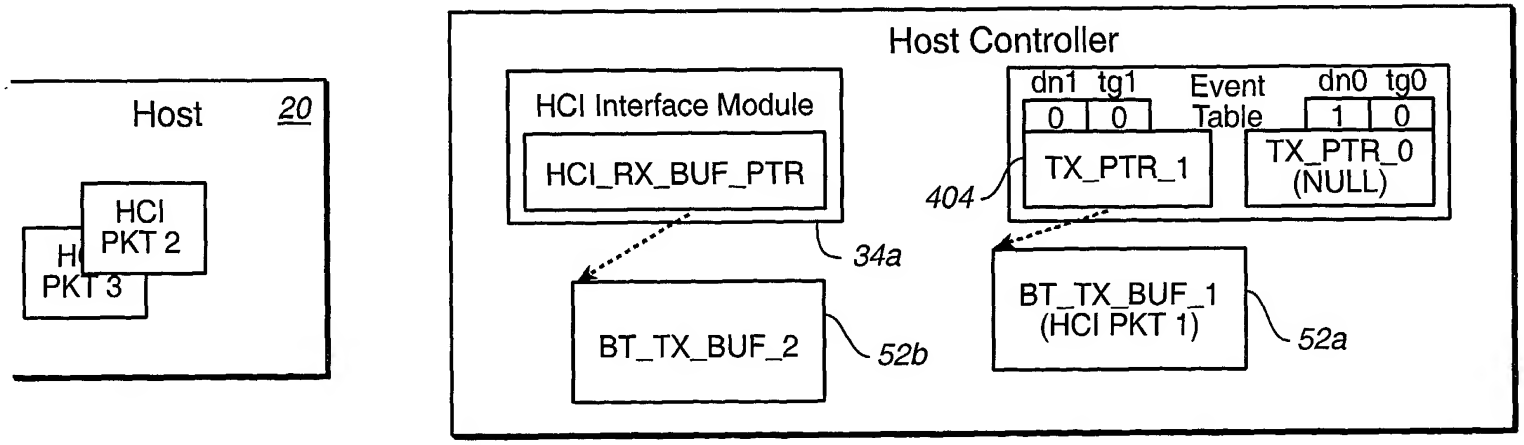


FIG._36D

Step 4: The Host Controller assigns another buffer 'BT_TX_BUF_2' to receive the HCI packet.



U.S. Patent Application Serial No. 10/052,877
Inventors: MIN-SHIN MA and ALLAN JON FLIPPIN
For: BLUETOOTH BASEBAND CONTROLLER
Sheet 27 of 45 Attorney Docket No.: M-10394-1P US

Step 5: While the Bluetooth Module is sending the HCI packet 1, the HCI Interface Module is receiving the HCI packet 2.

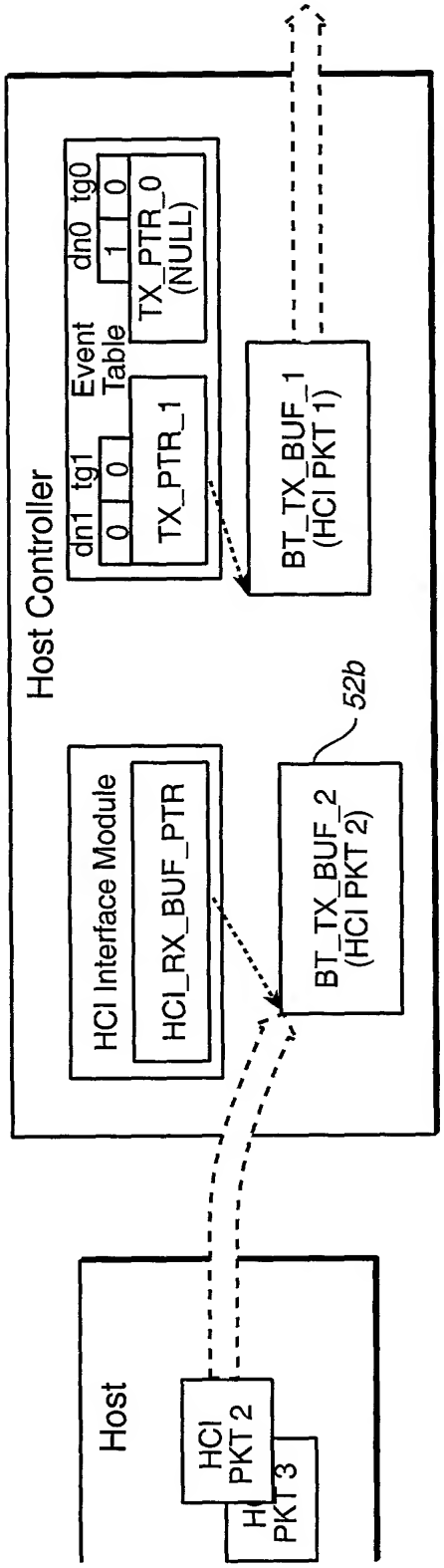


FIG._36E

Step 6: Assuming that the HCI packet 1 is sent before the HCI packet 2 is received, the buffer 'BT_TX_BUF_1' is released.

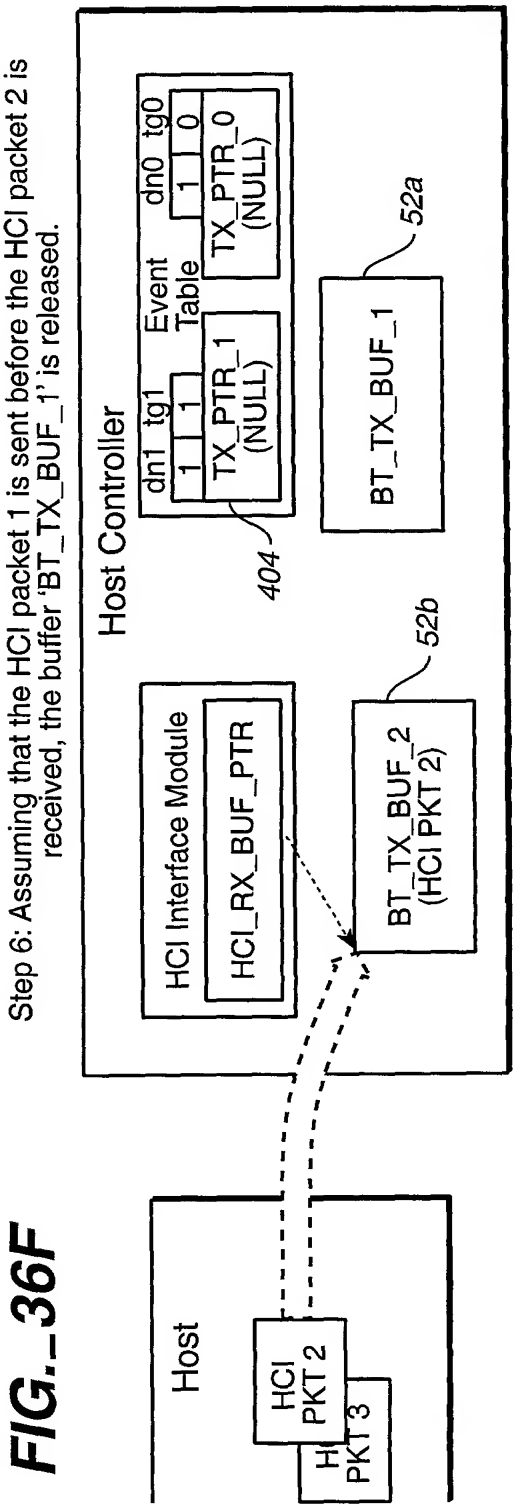


FIG._36F

FIG._36G

Step 7: After the HCI packet 2 has been received, the buffer 'BT_TX_BUF _2' is pointed by 'TX_PTR_0'.

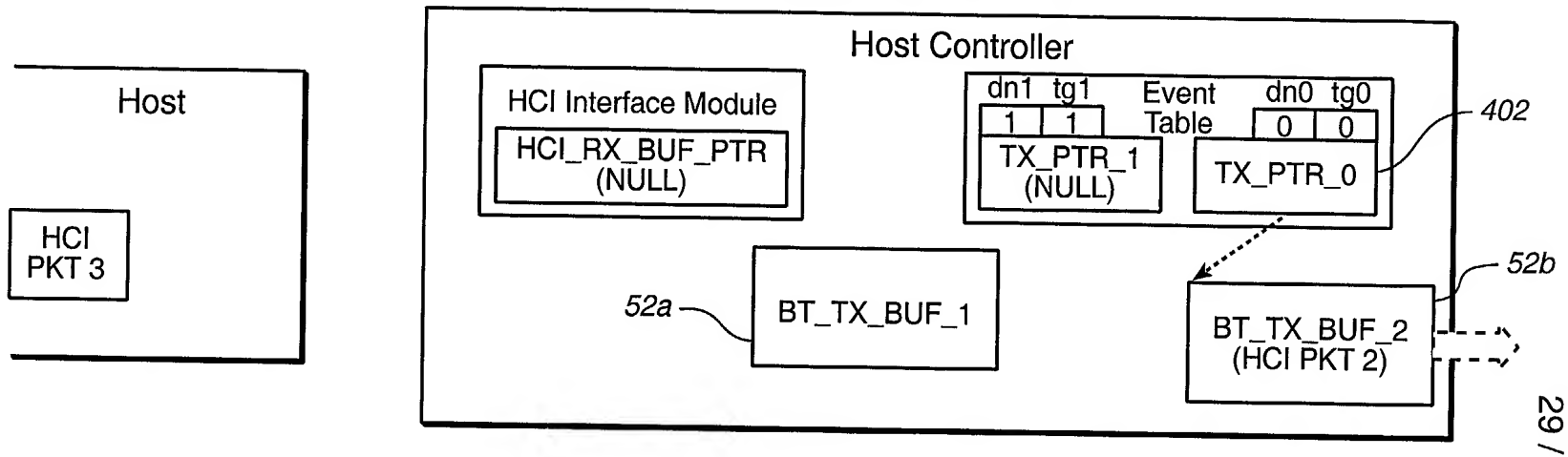


FIG._36H

Step 8: The free buffer 'BT_TX_BUF_1' is assigned to the HCI Interface Module again to receive another HCI packet.

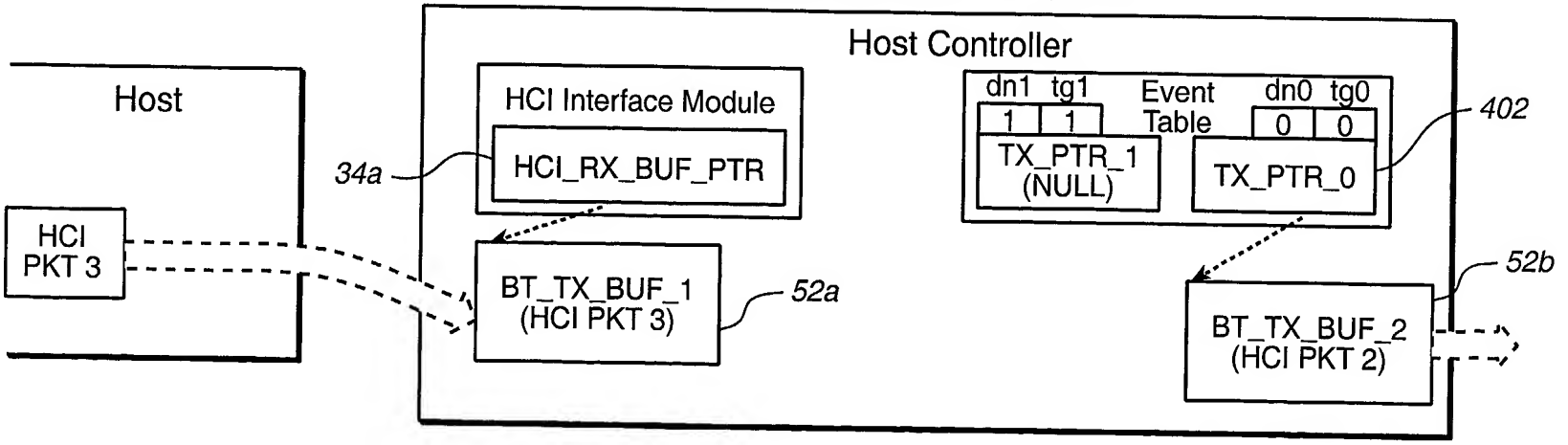


FIG._36I

Step 9: Assuming that the HCI packet 3 is received before the HCI packet 2 is sent, 'TX_PTR_1'points to buffer 'BT_TX_BUF_1'.

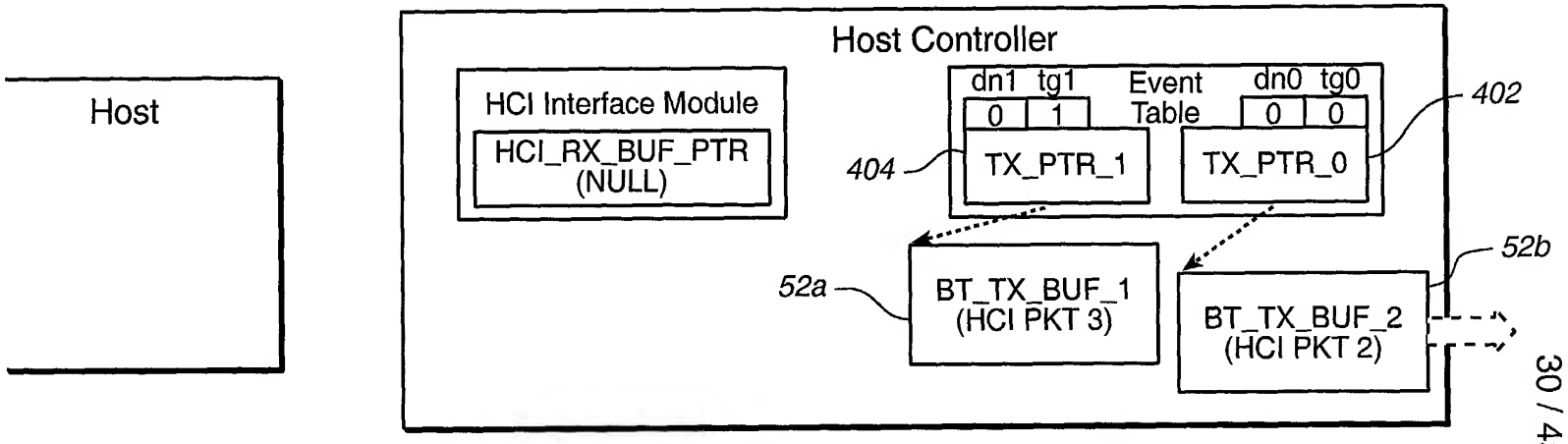
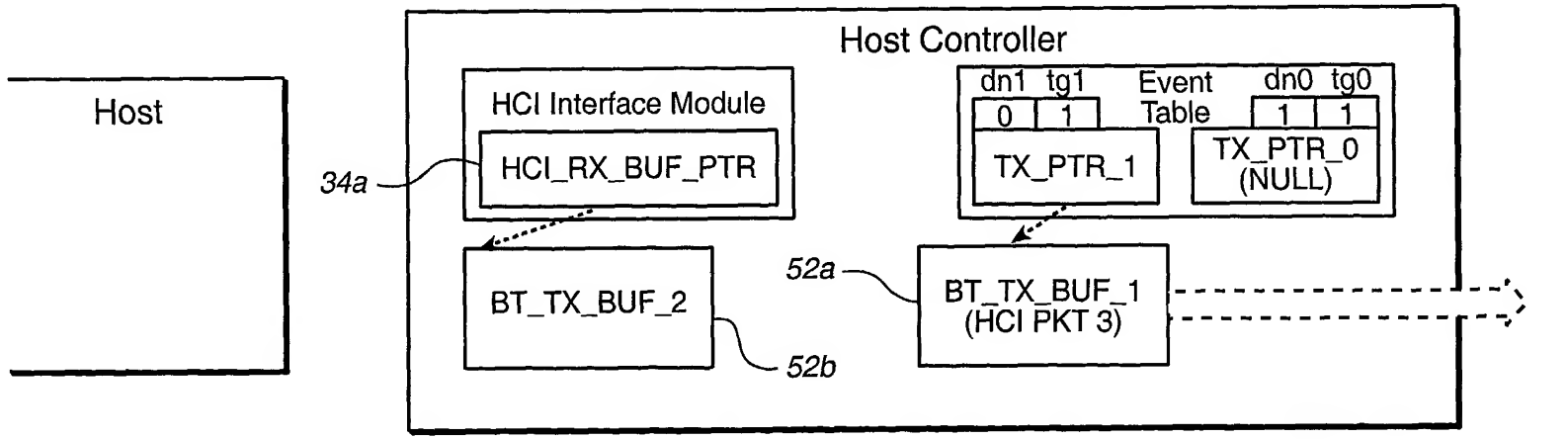


FIG._36J

Step 10: The free buffer 'BT_TX_BUF_2' is assigned to the HCI Interface Module again to receive another HCI packet.



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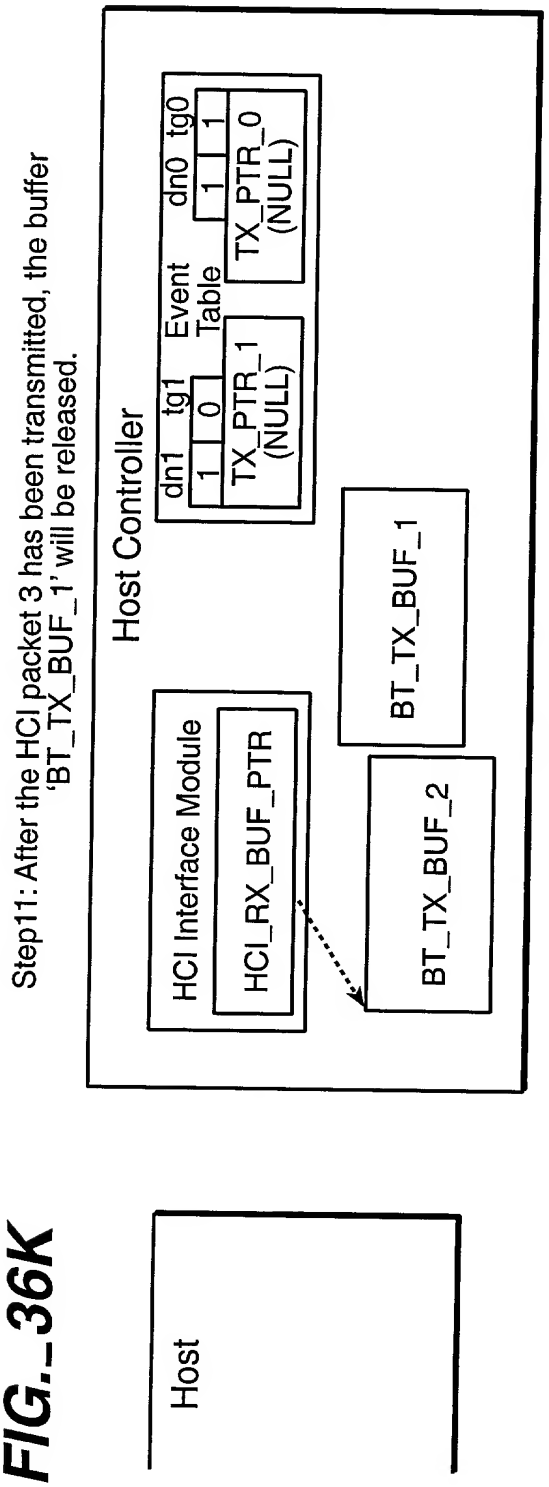


FIG._36K

FIG._37A

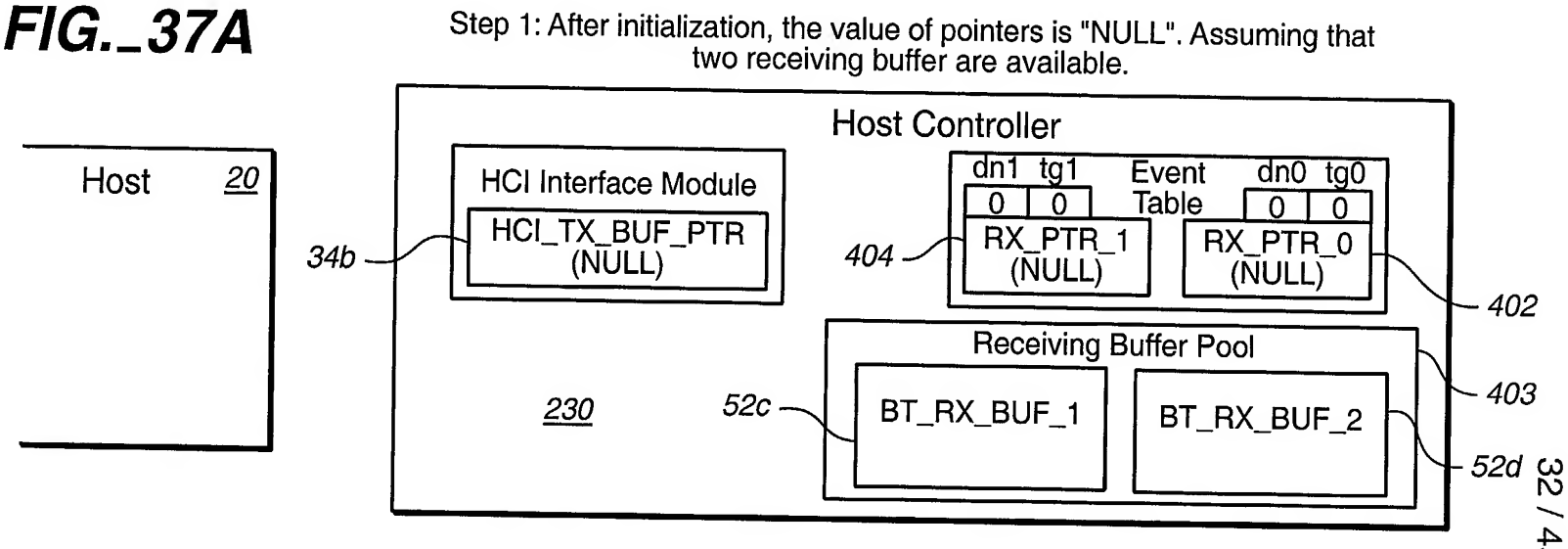


FIG._37B

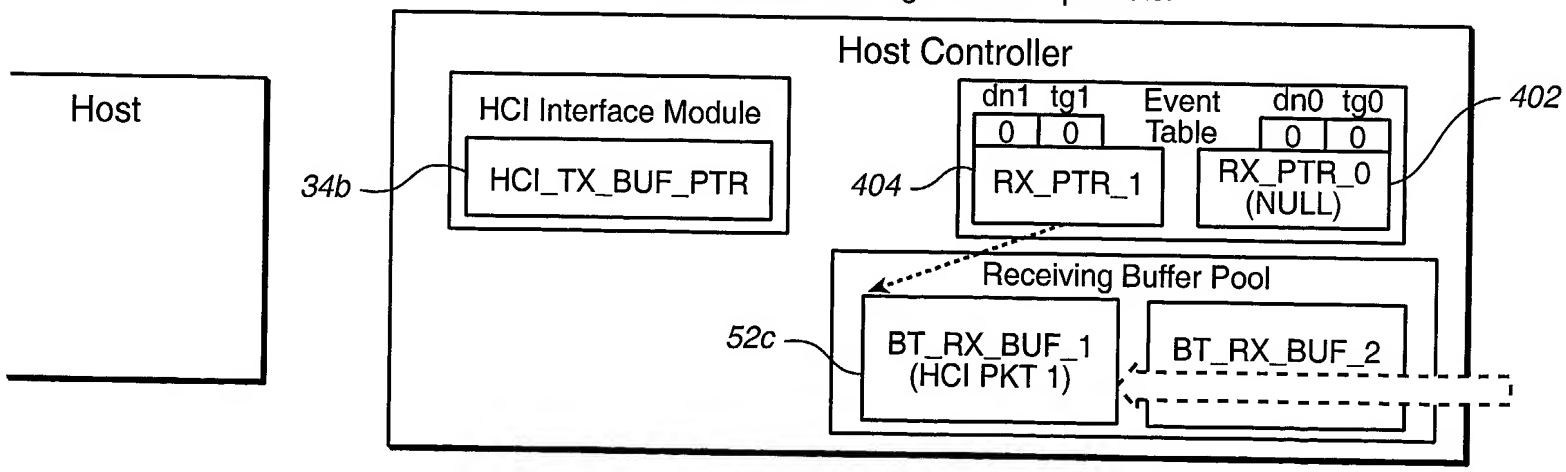


FIG._37C

Step 3: The buffer 'BT_TX_BUF_1' is released when any one of the three buffer releasing conditions is detected.

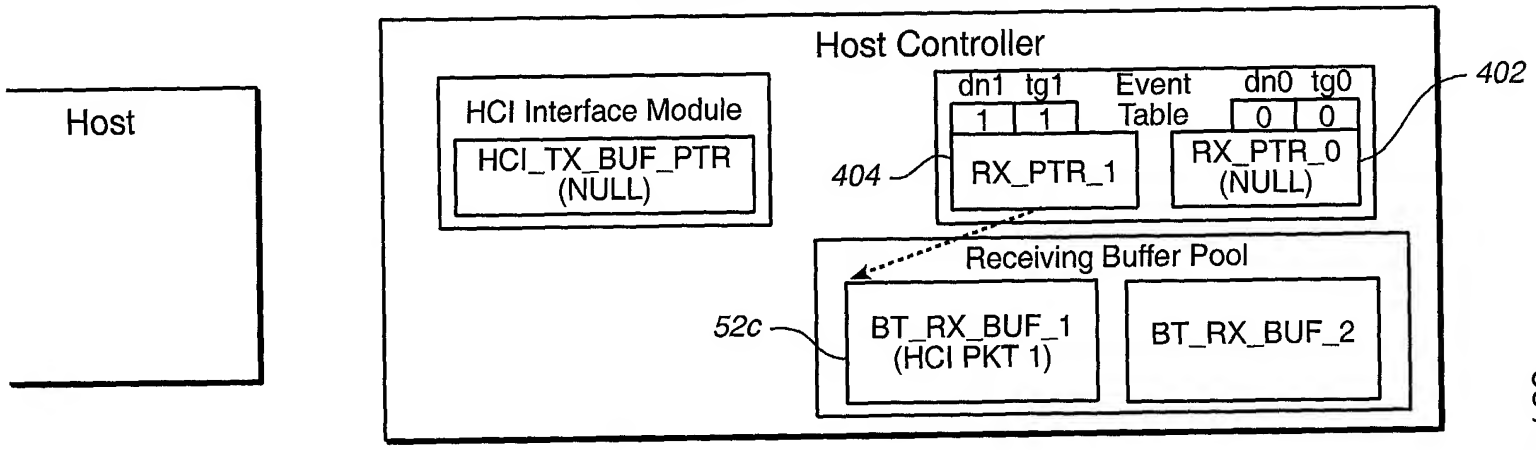
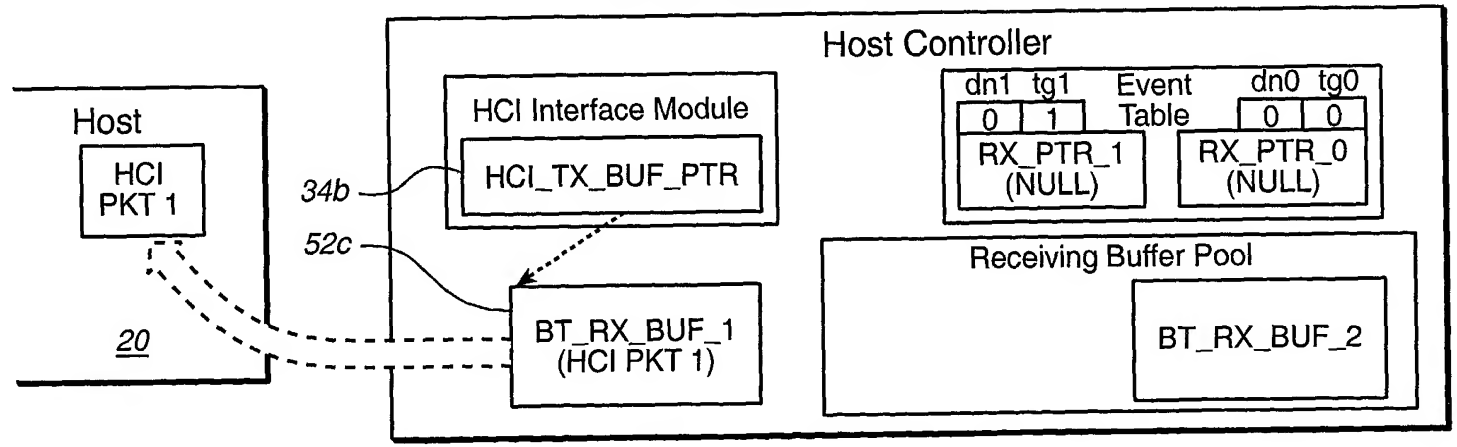


FIG._37D

Step 4: Firmware releases this buffer 'BT_TX_BUF_1' and sends it to the HCI Interface Module. Then sets the done bit to 0.



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Inventors: MIN-SHIN MA and ALLAN JON FLIPPIN
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FIG._37E

Step 5: After the HCI packet 1 is sent to the Host, buffer 'BT_RX_BUF_1' is released and put back to the receiving buffer pool.

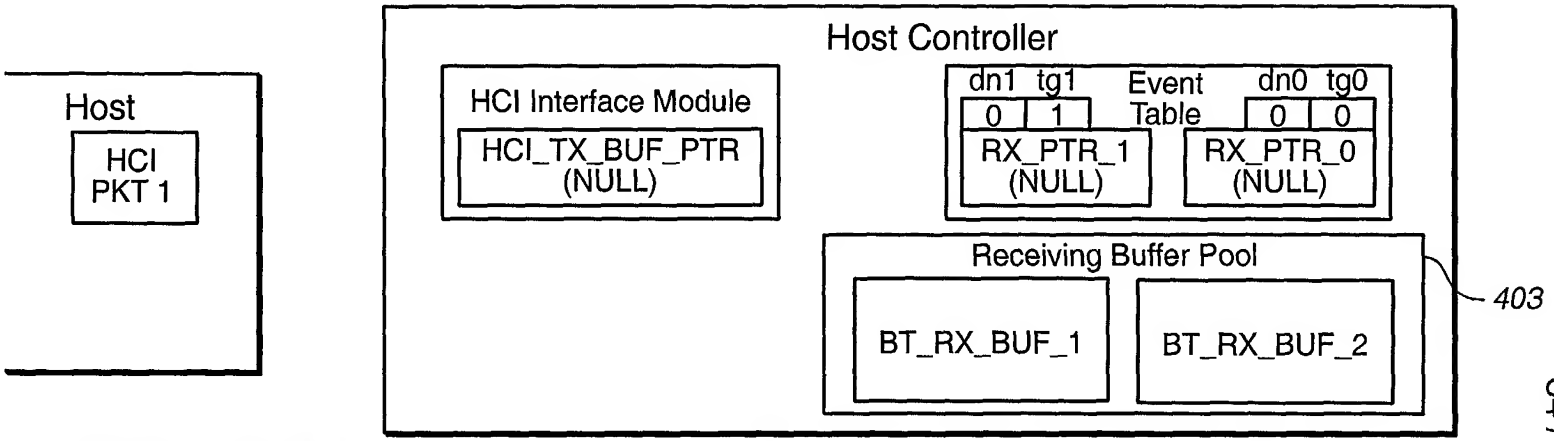
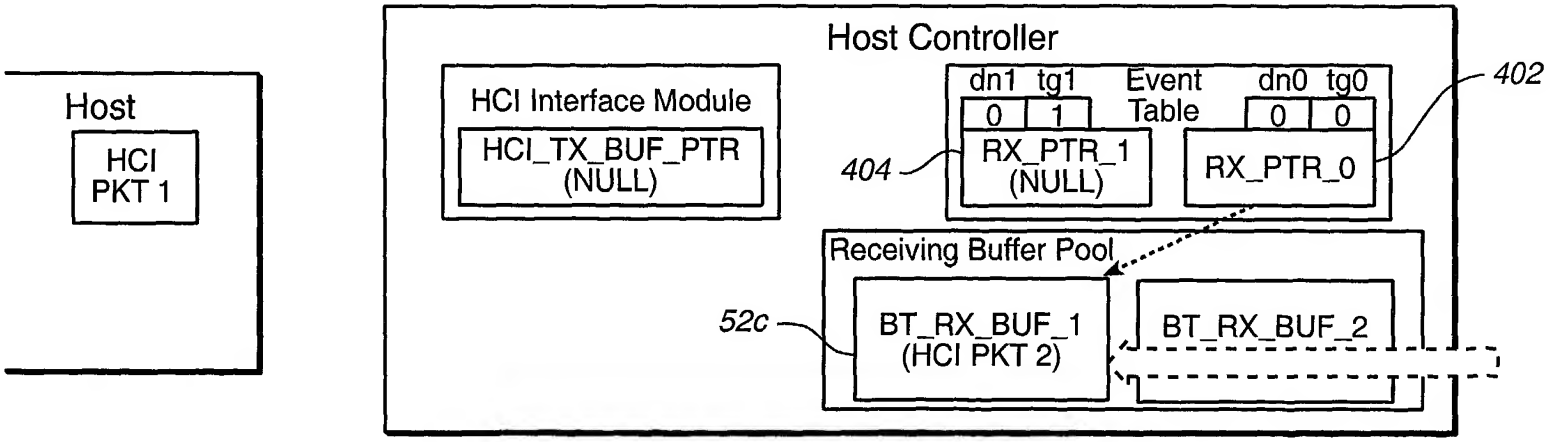


FIG._37F

Step 6: The Bluetooth Module assigns buffer 'BT_RX_BUF_1' to receive the incoming Bluetooth packets.



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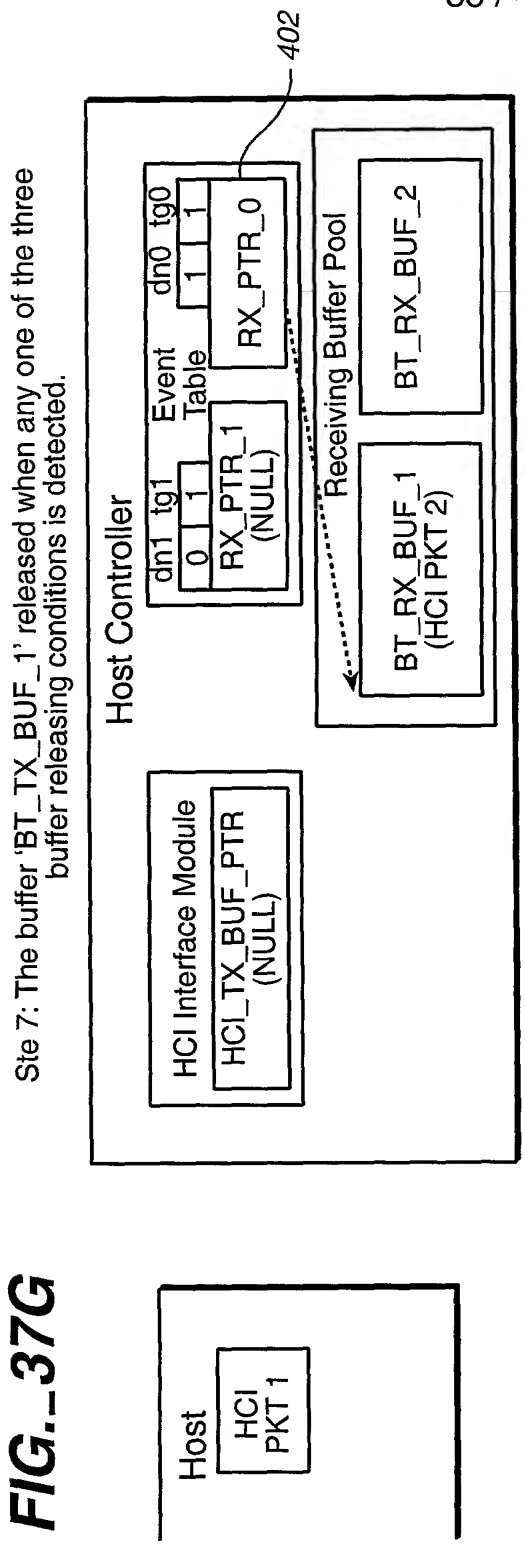


FIG._37G

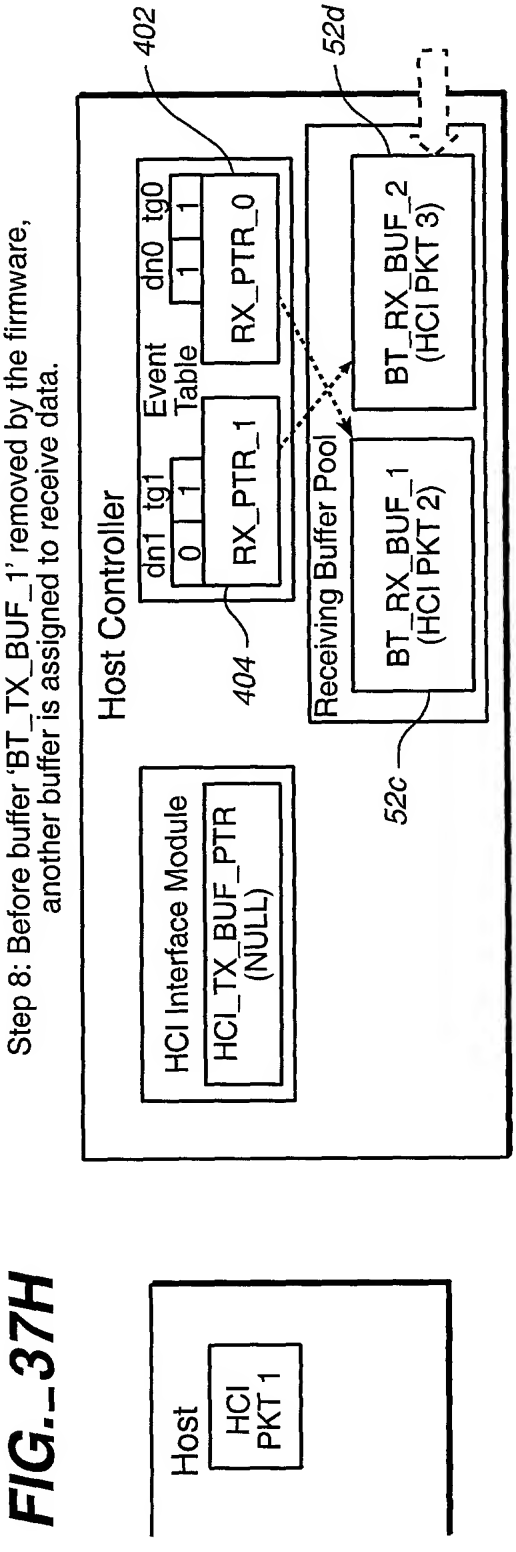


FIG._37H

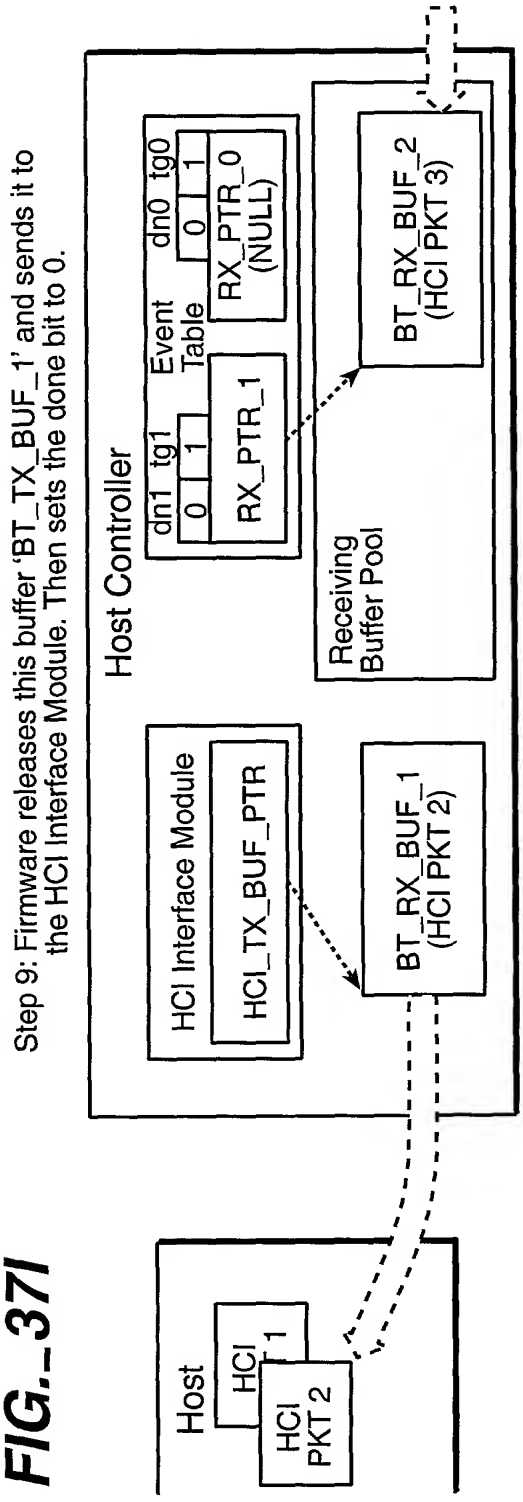


FIG._37I

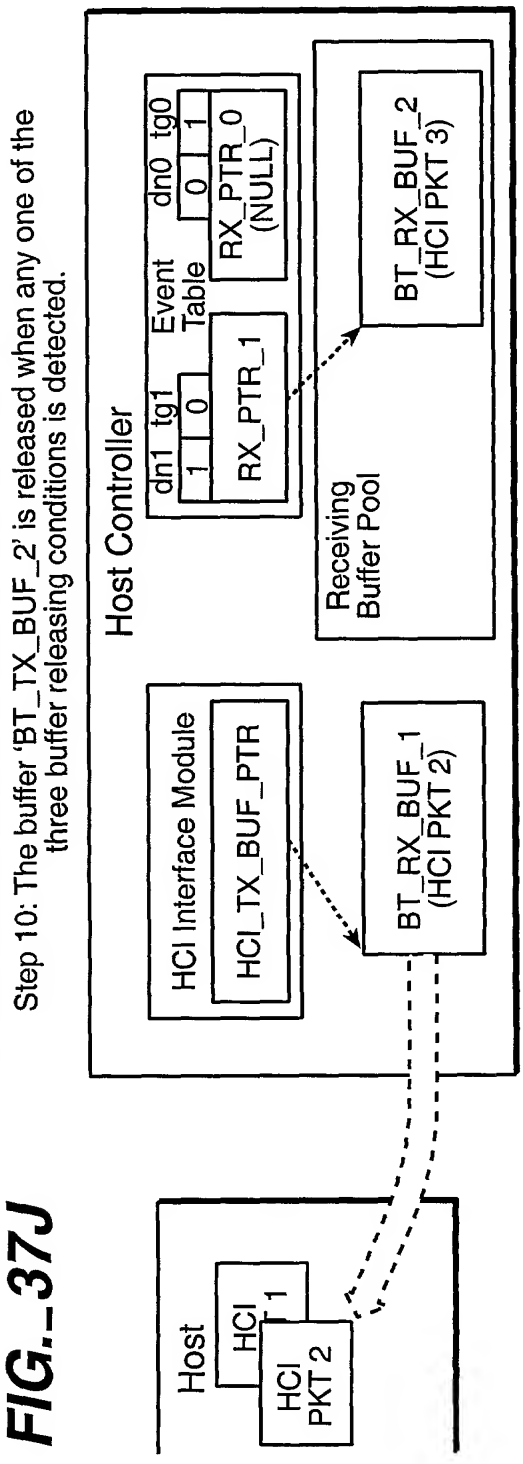


FIG._37J

FIG._37K

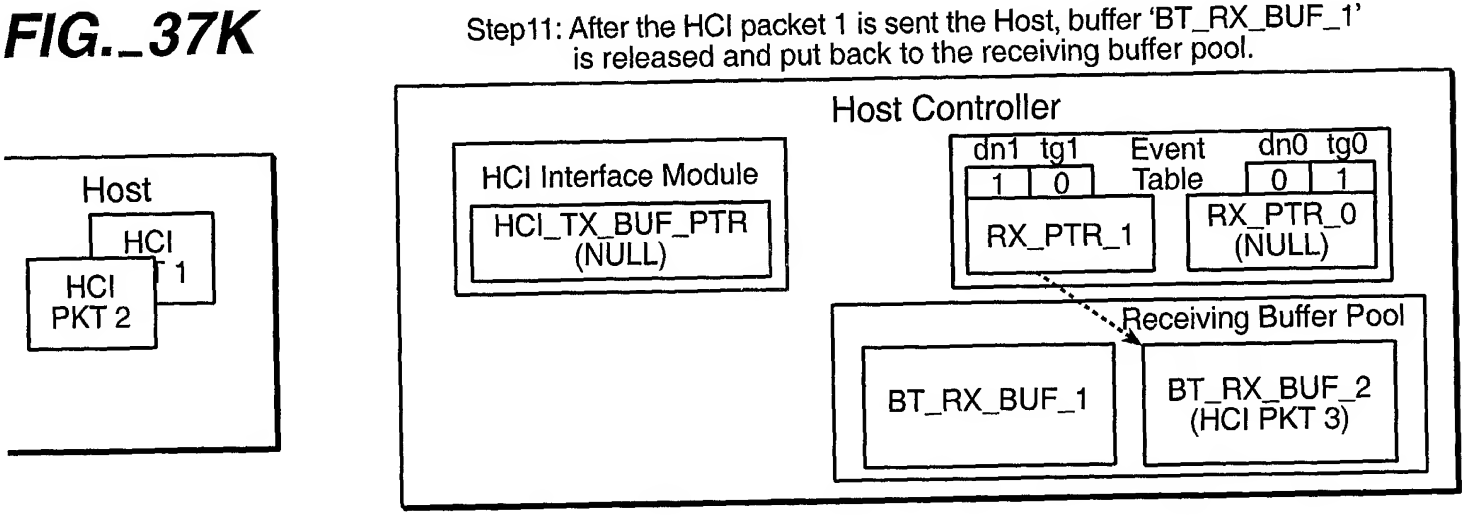
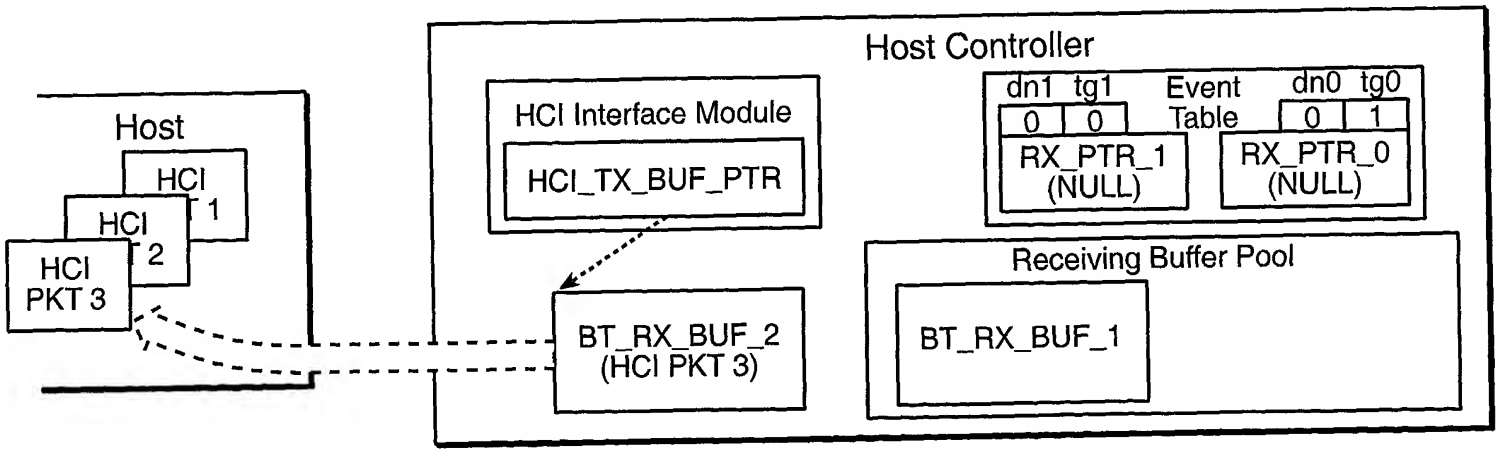


FIG._37L



Dua Pointer Buffer Scheme 1: Hardware implementation

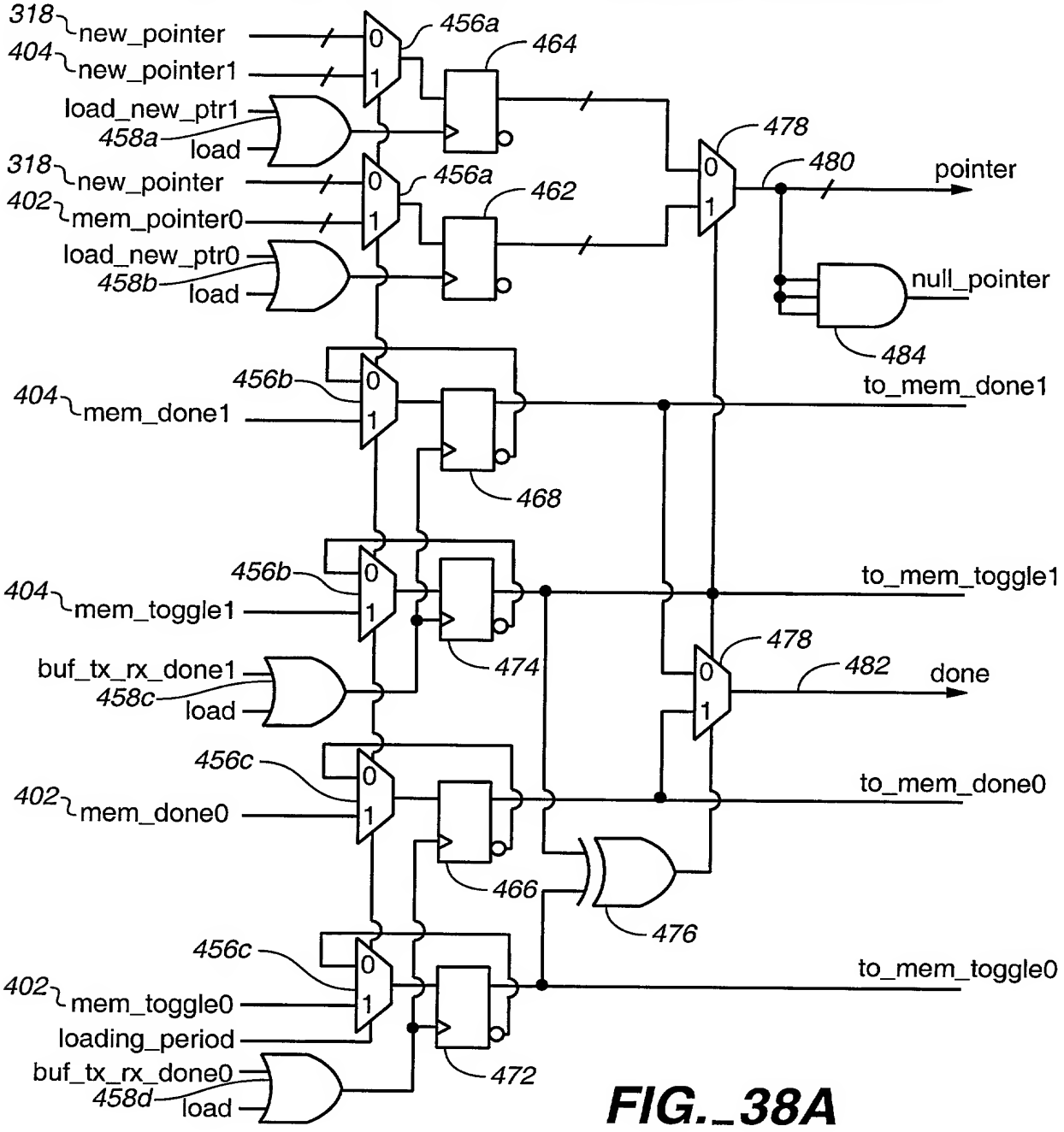


FIG._38A

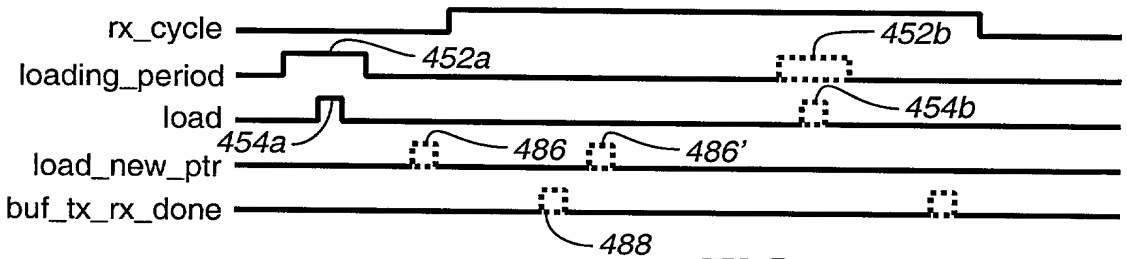


FIG._38B

Duel Pointer Buffer Scheme 1: Firmware implementation

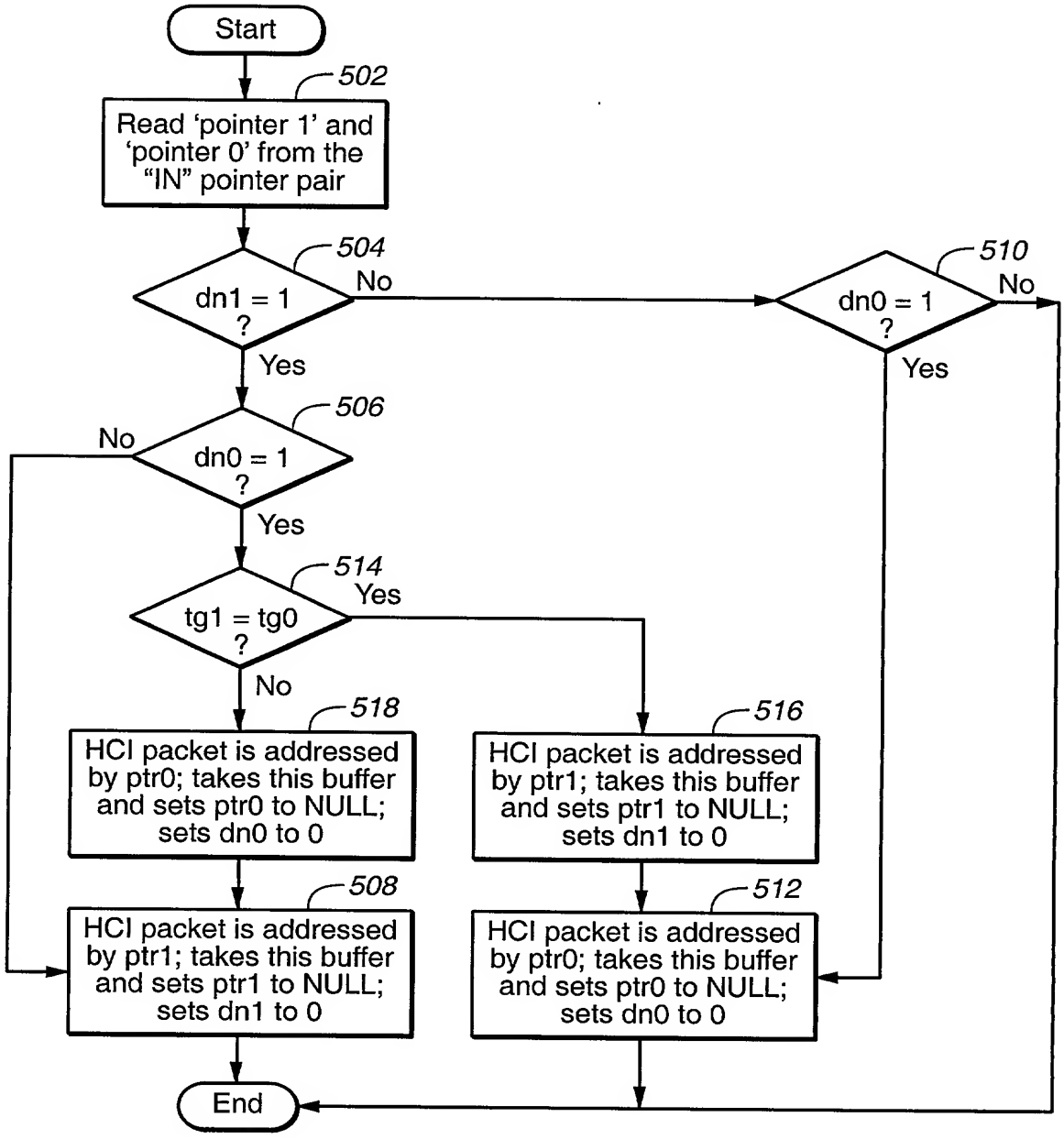


FIG._39

Duel Pointer Buffer Scheme 1: Firmware implementation

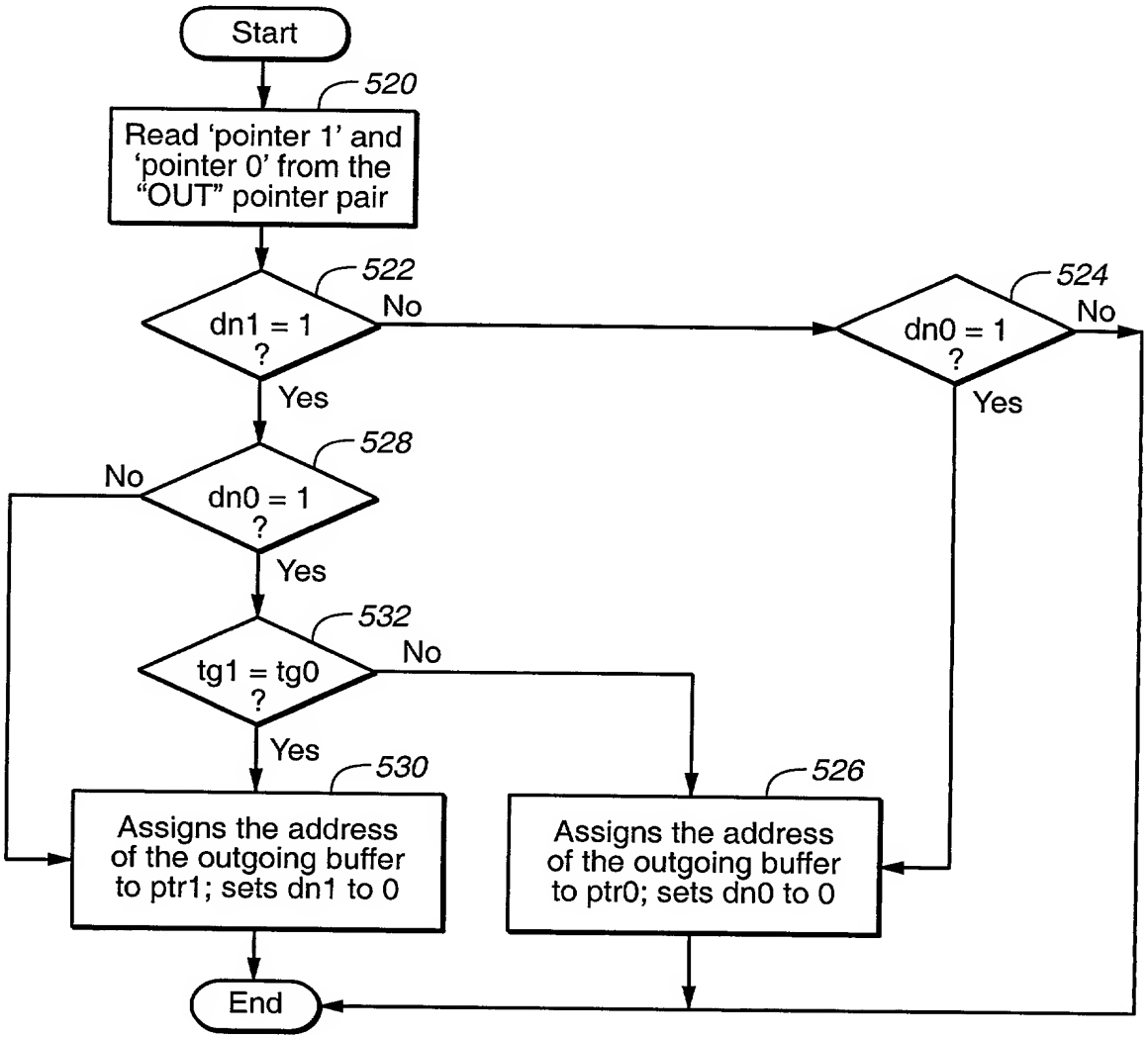


FIG._40

Duel Pointer Buffer Scheme 1: Firmware implementation

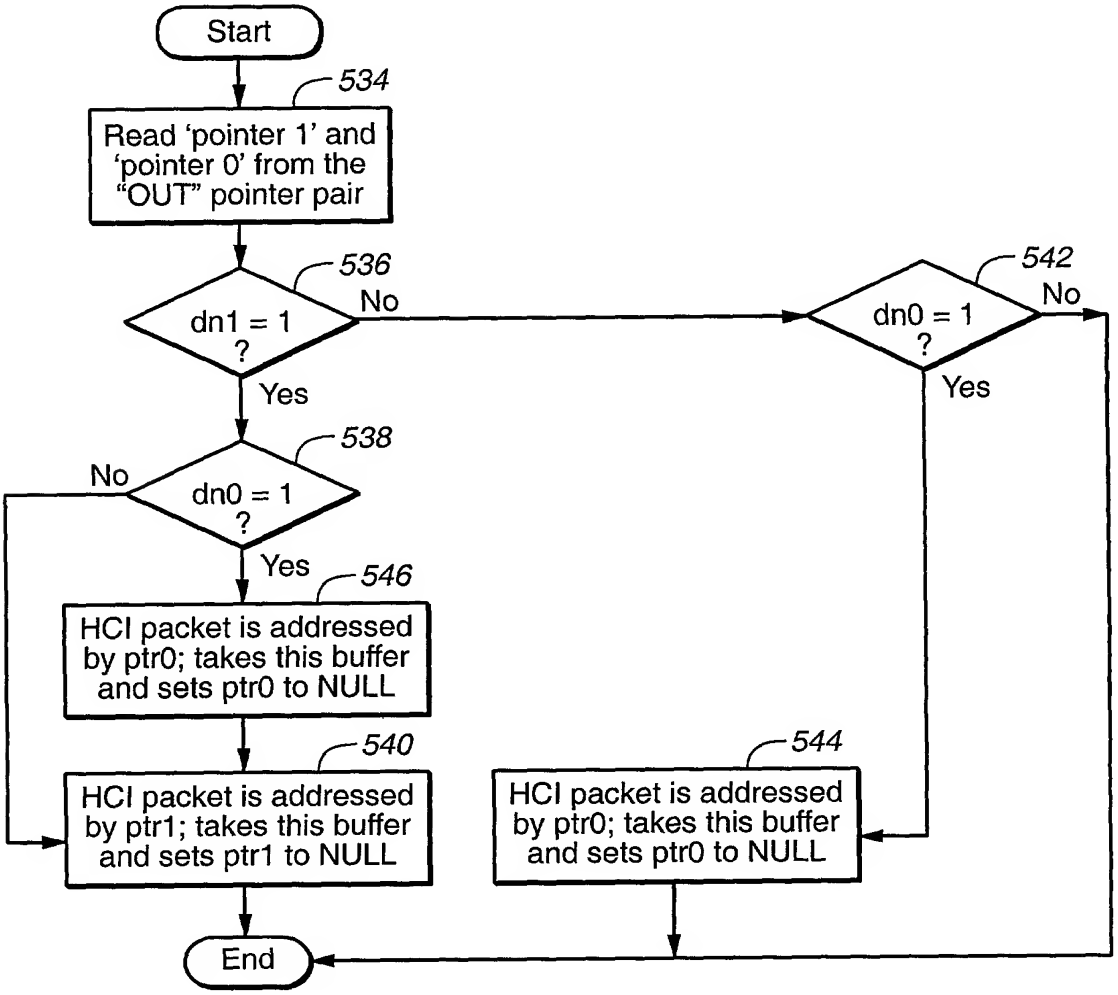


FIG._41

ACL RX precedure

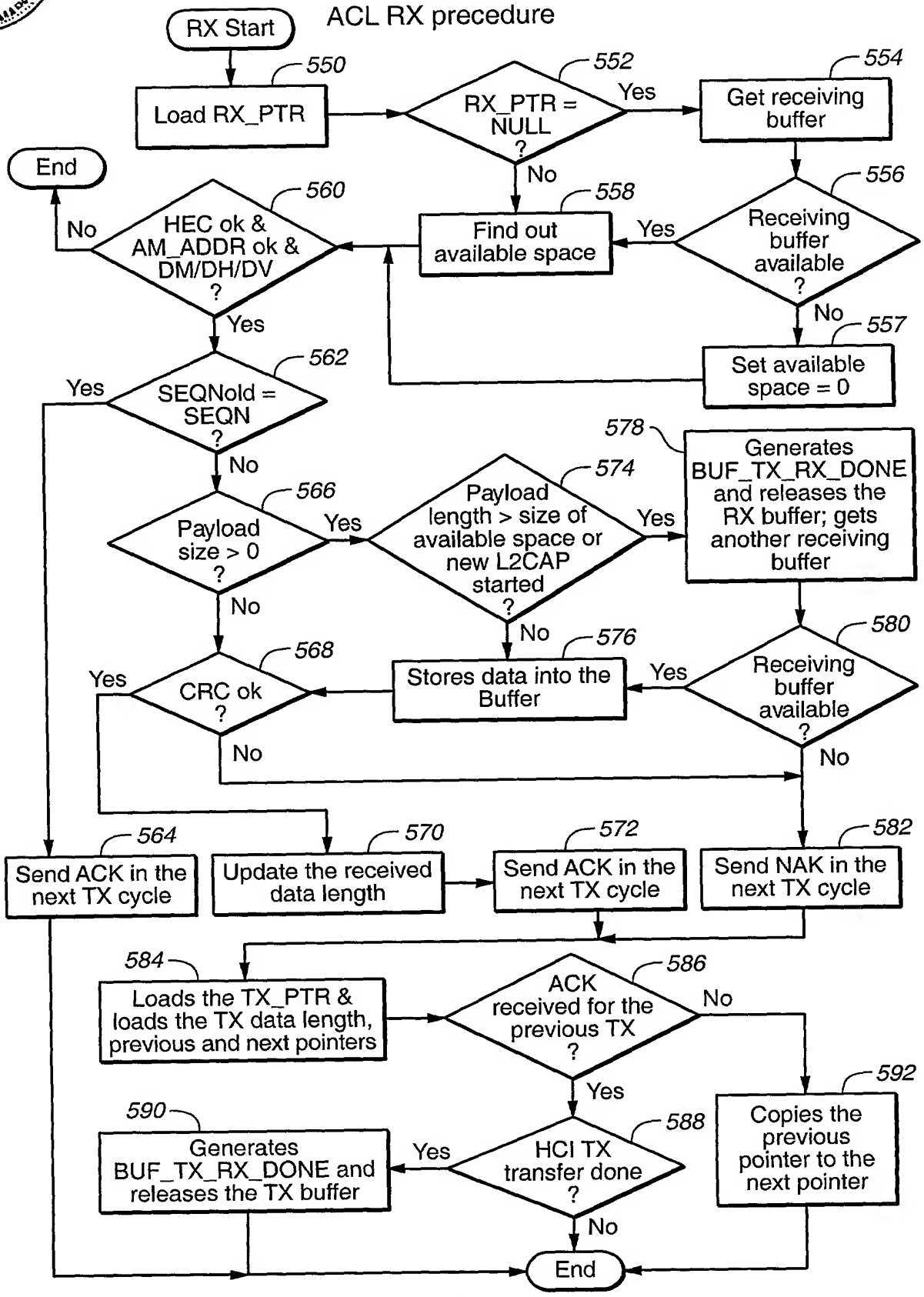


FIG._42

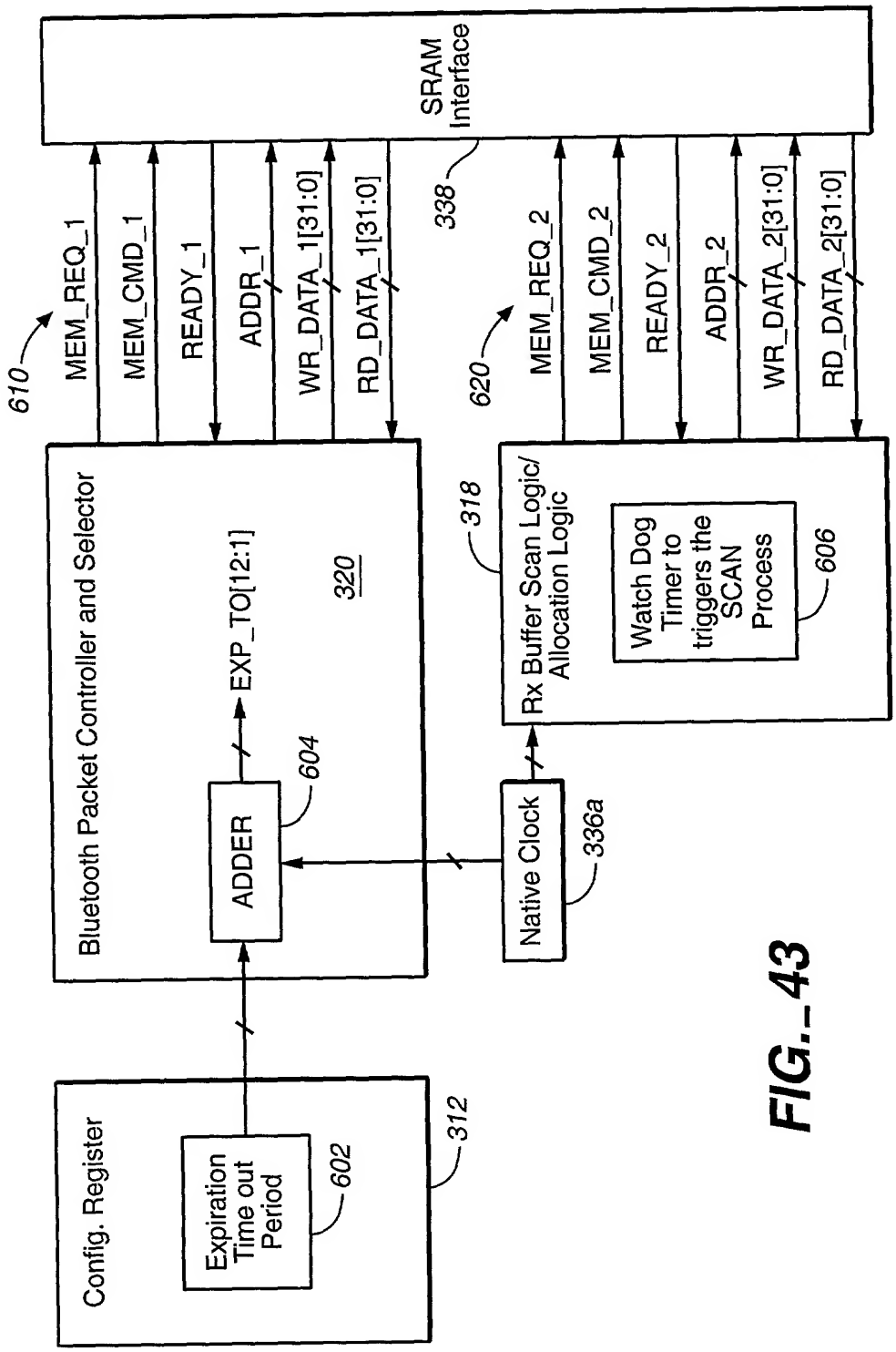


FIG._43

ACL RX Buffer is released due to expiration time-out

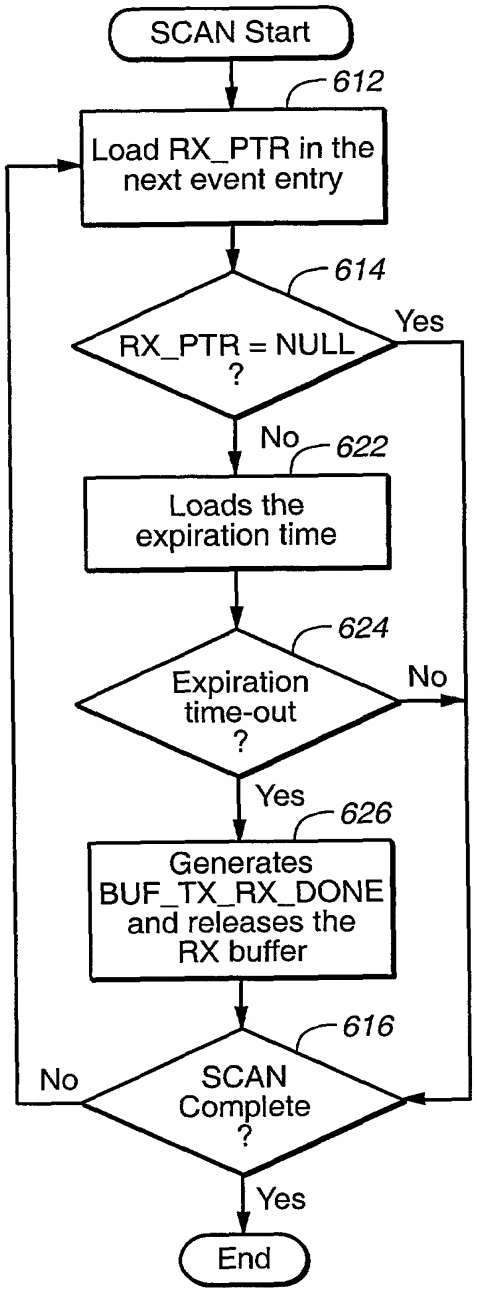


FIG._44

Scheduler - Scheduling priority of ACL links in master mode

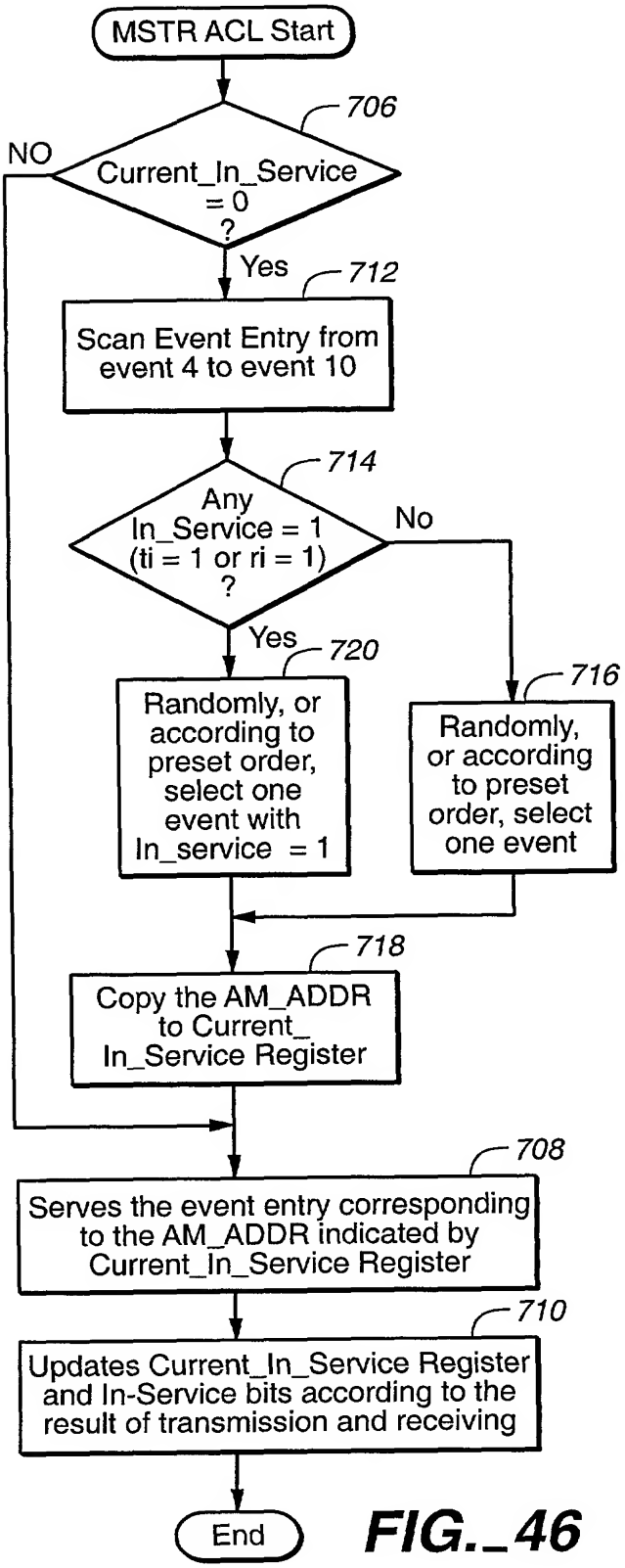


FIG._46

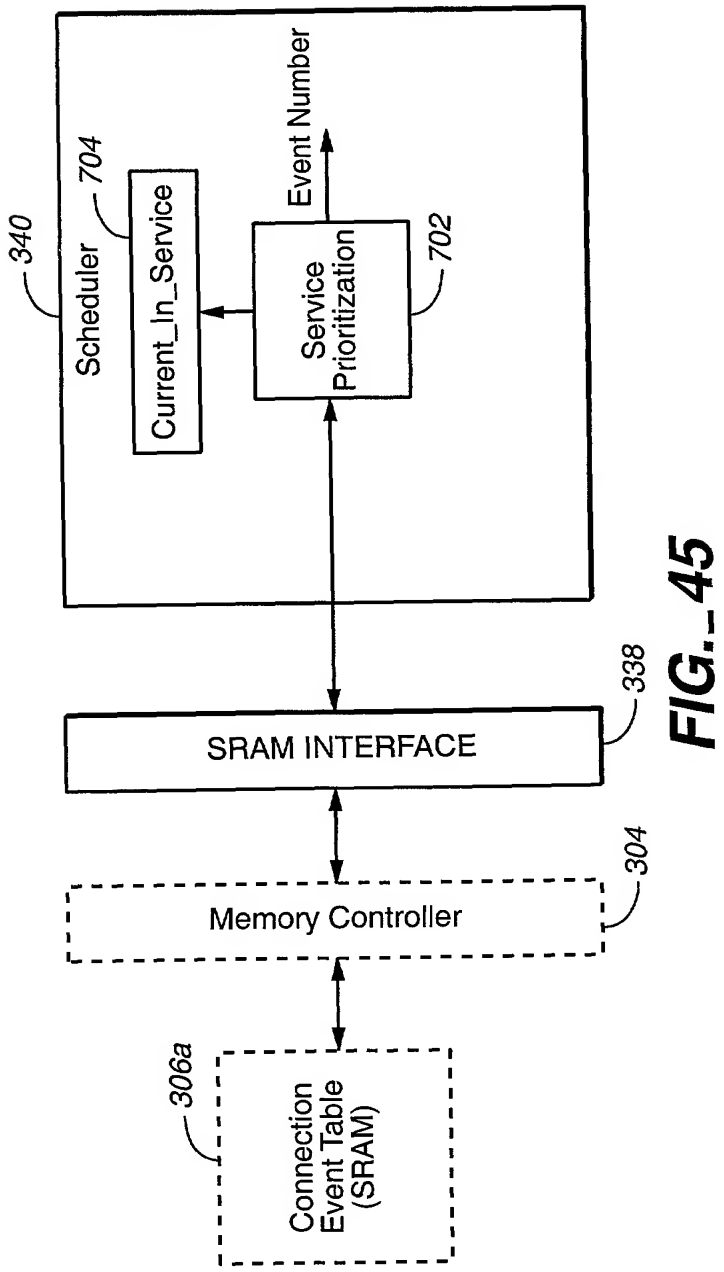


FIG._45